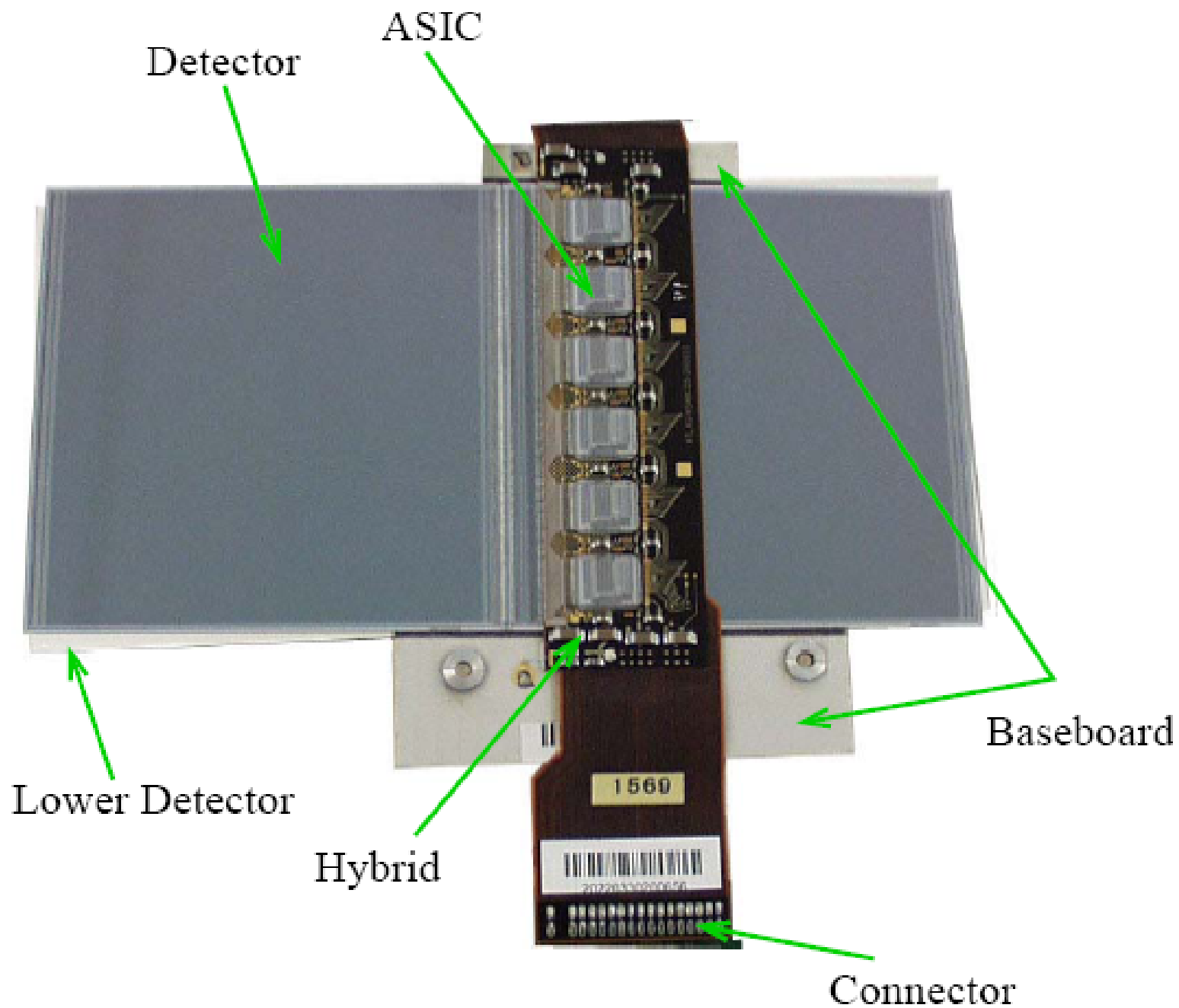


SctRodDaq

CGL



The ASICs are called “ABCD”s

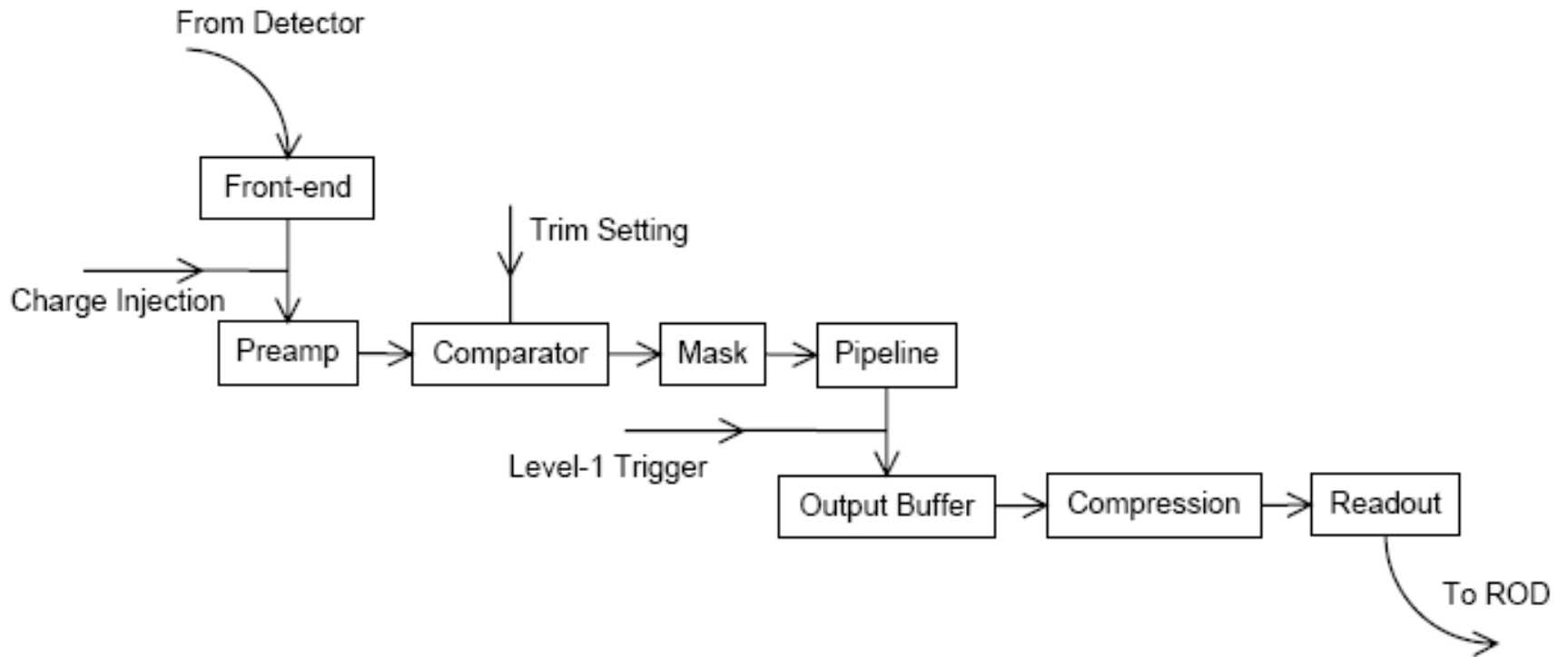
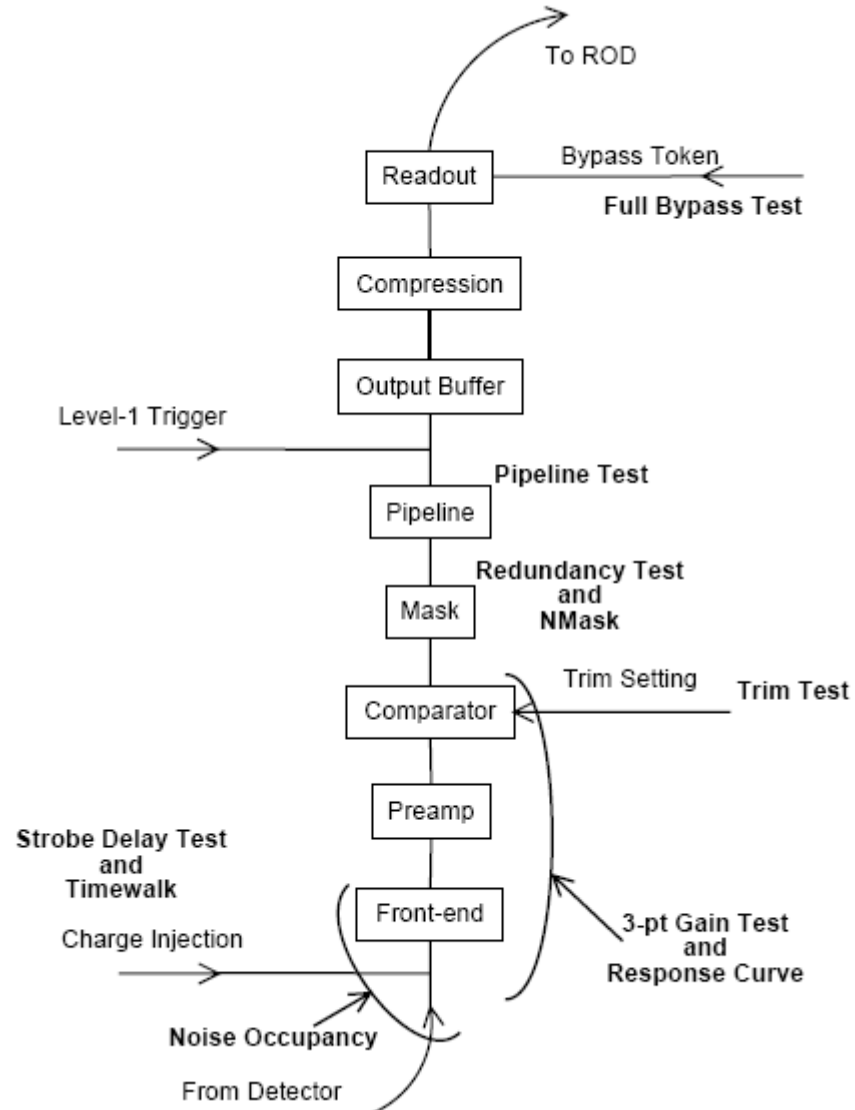
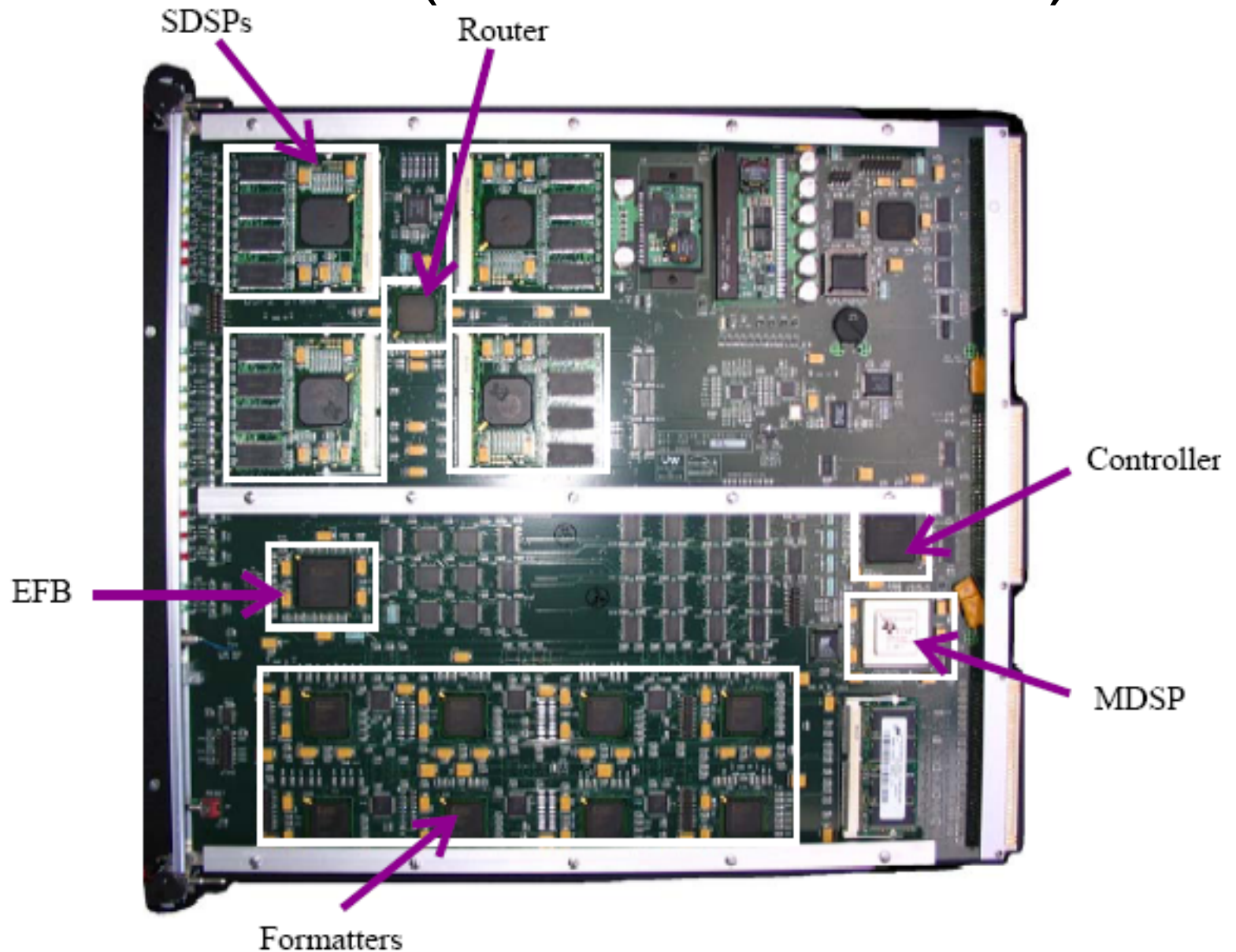


Figure 3.5: The components of the ABCD chip

Where the tests come in



A "ROD" (Read Out D*****)



A Rod Crate:

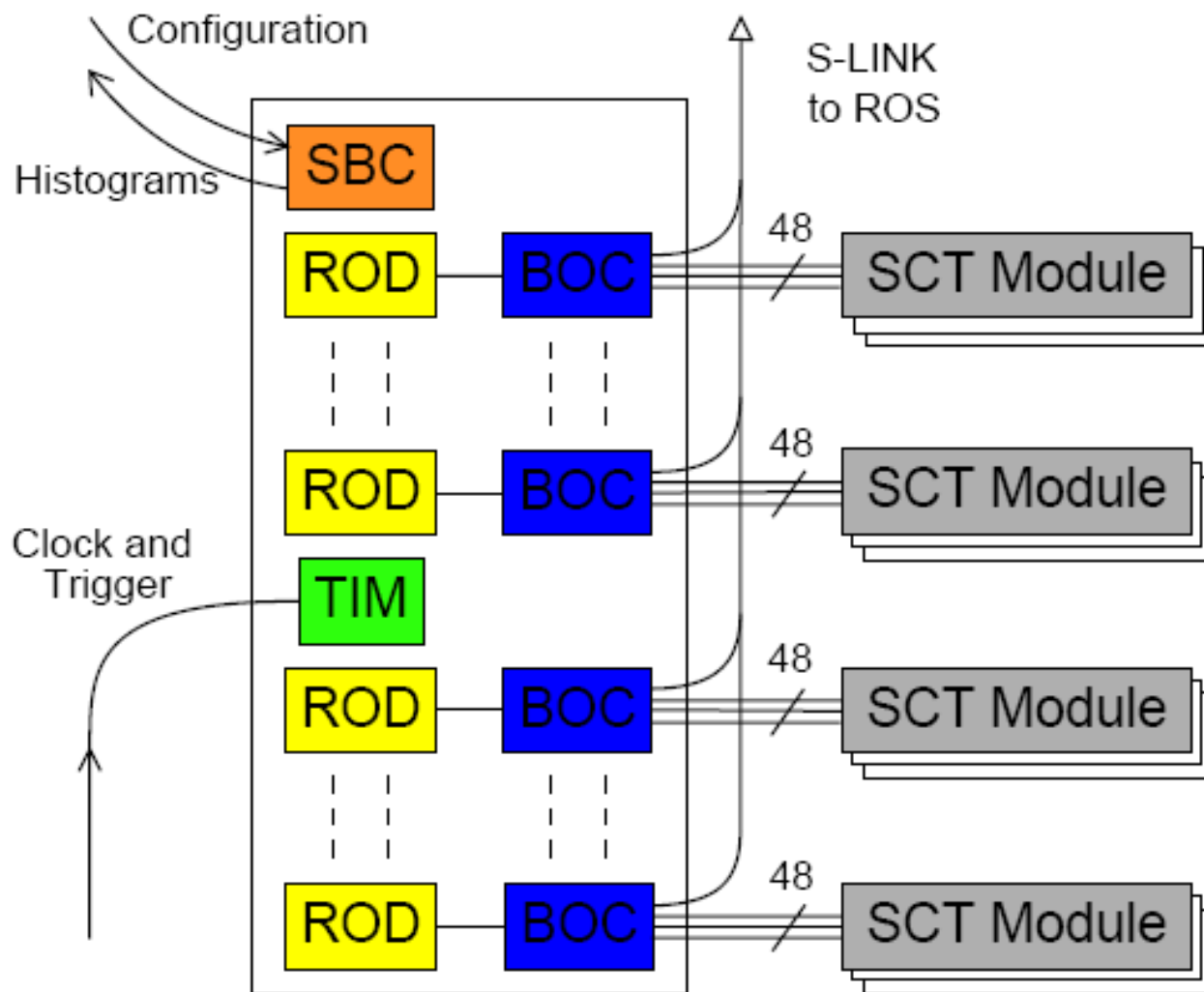
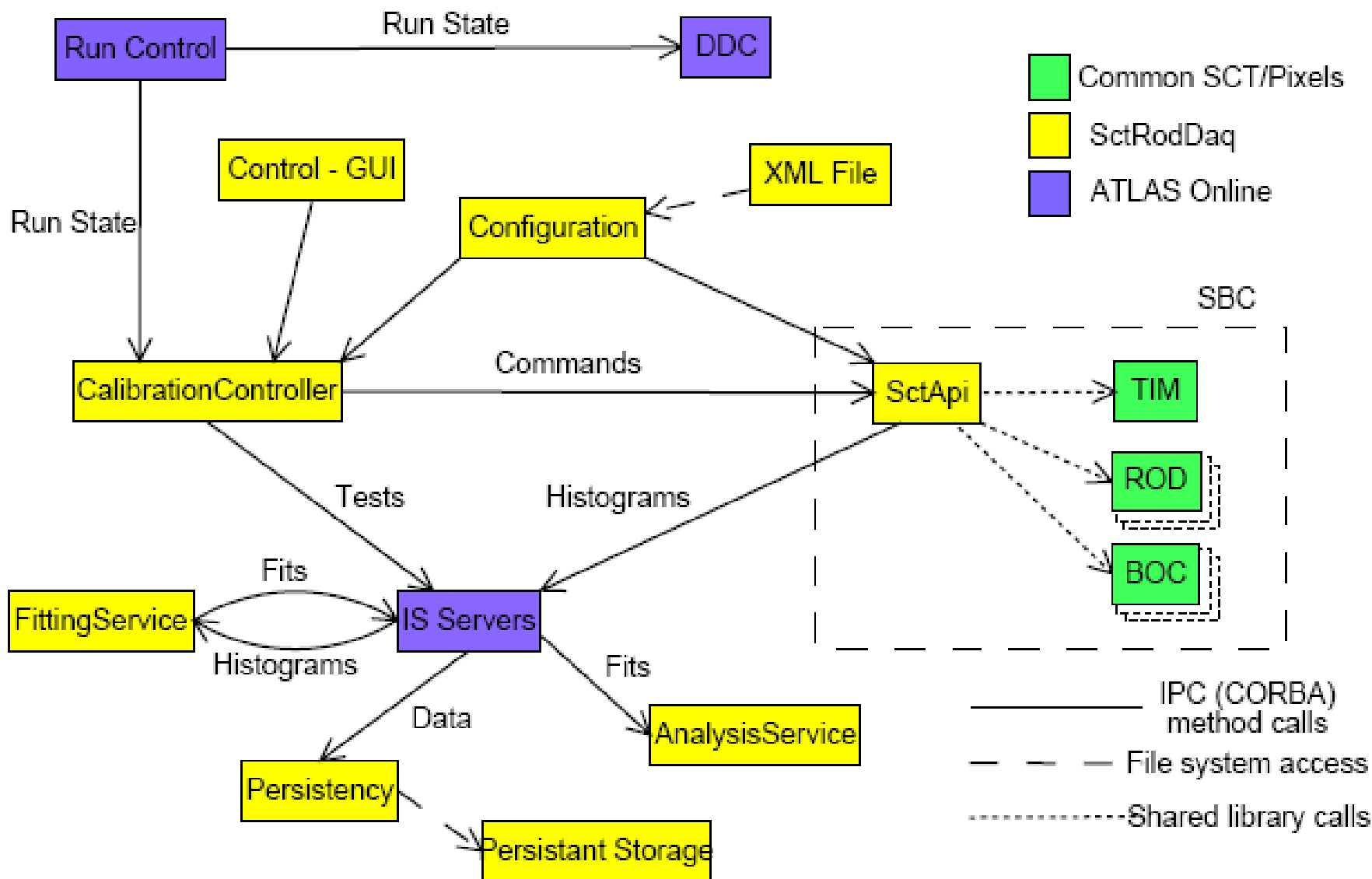
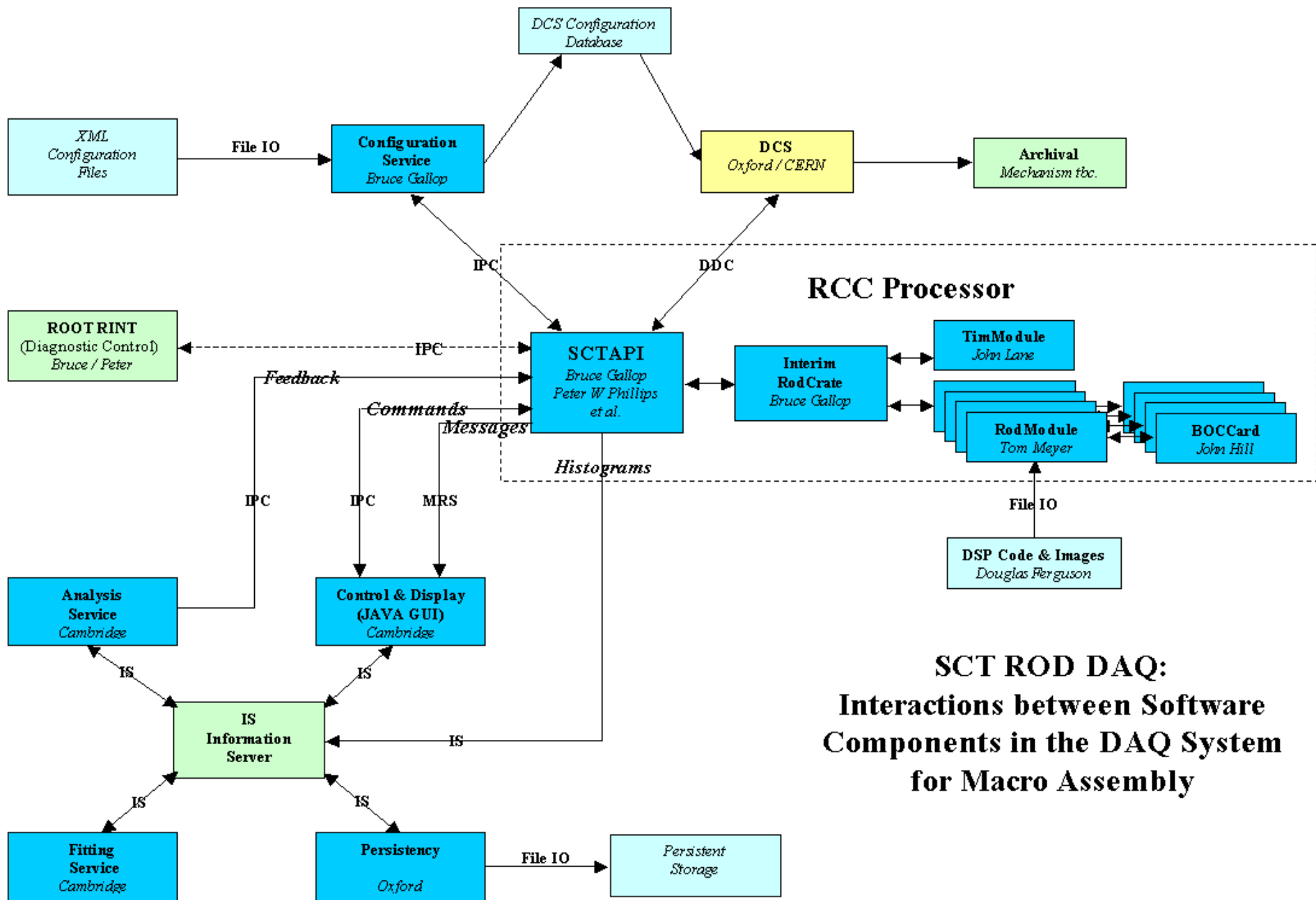


Figure 3.8: Schematic of the VME cards in a ROD crate, showing connections to the SCT modules and to the ROS which communicates with level 2 and the event builder

SctRodDaq – The software “Glue”





How user gets a calib histo

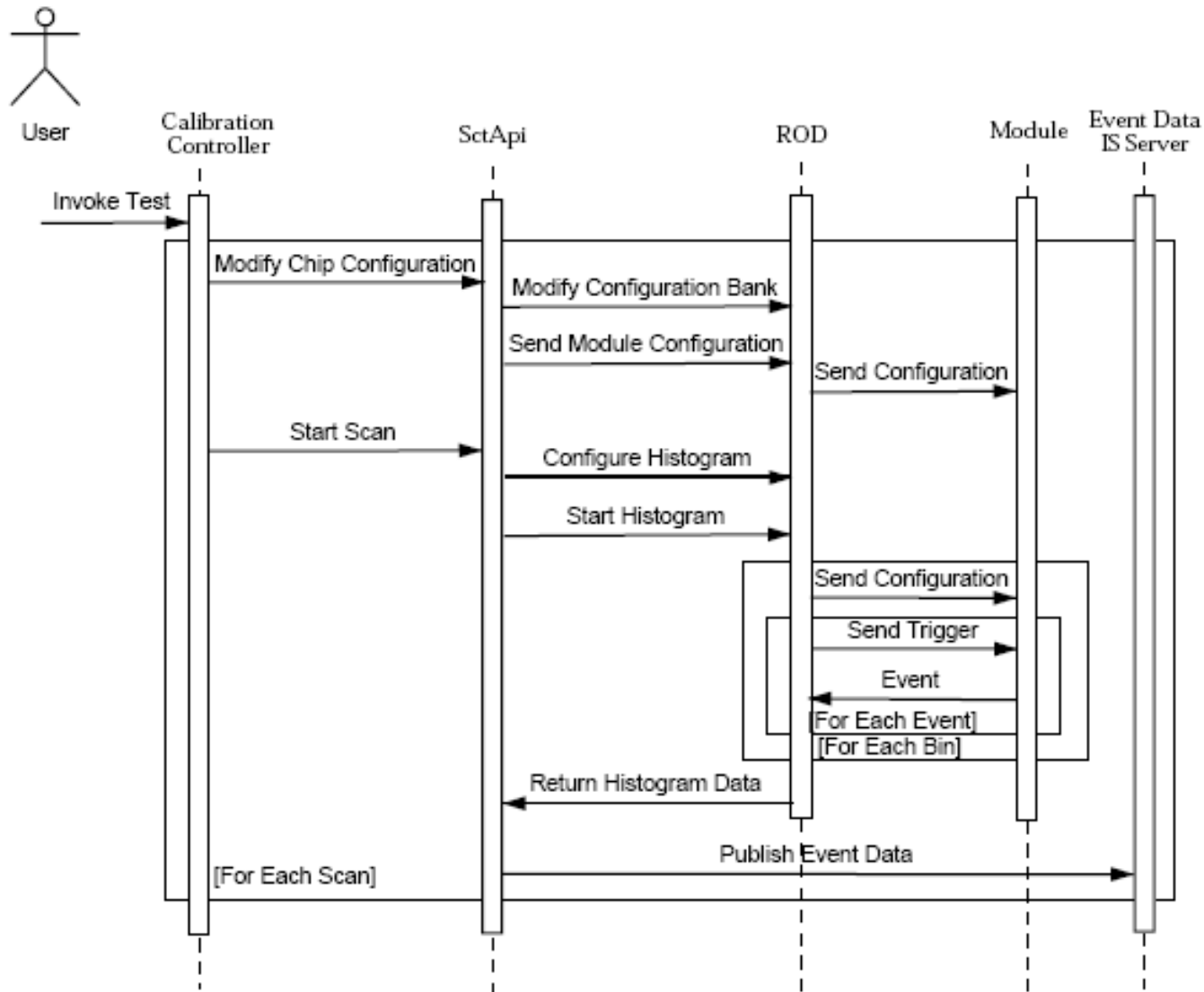


Figure 4.4: Sequence diagram showing the production of histogram data by the SctApi. The complete data is published to the Event Data IS Server. Further processing of this

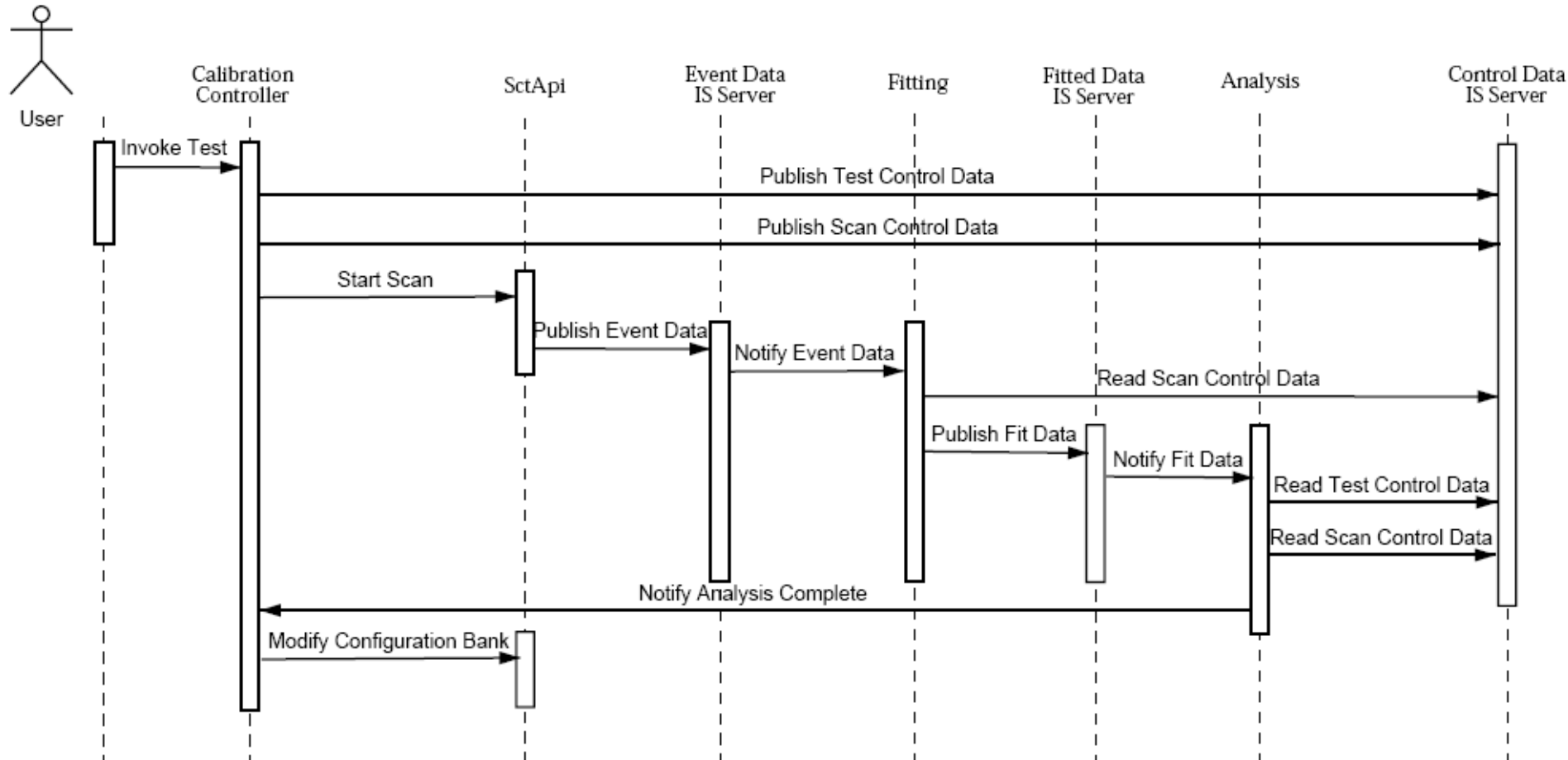
The Analysis Rollercoaster



Not like this:

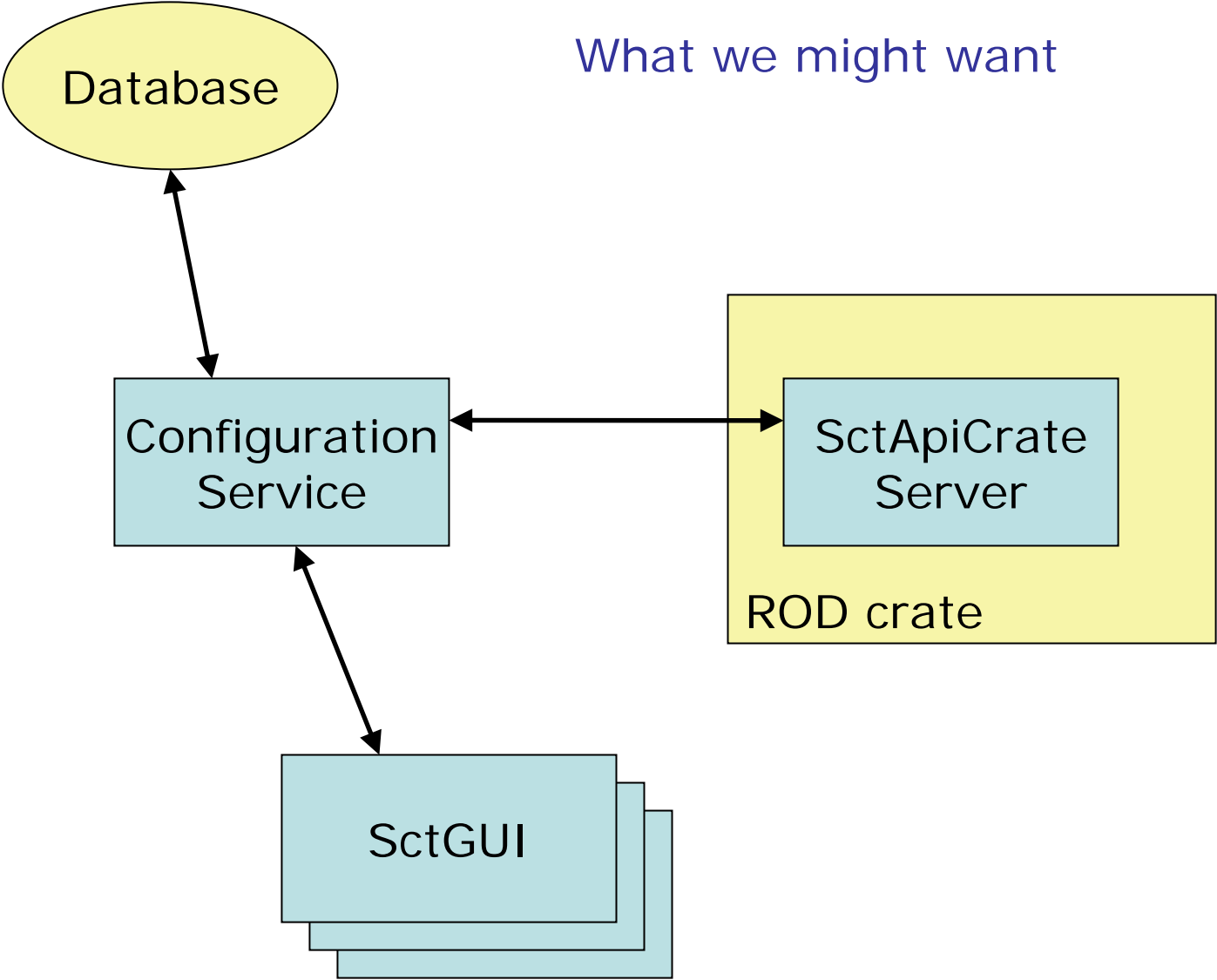


The Analysis Rollercoaster

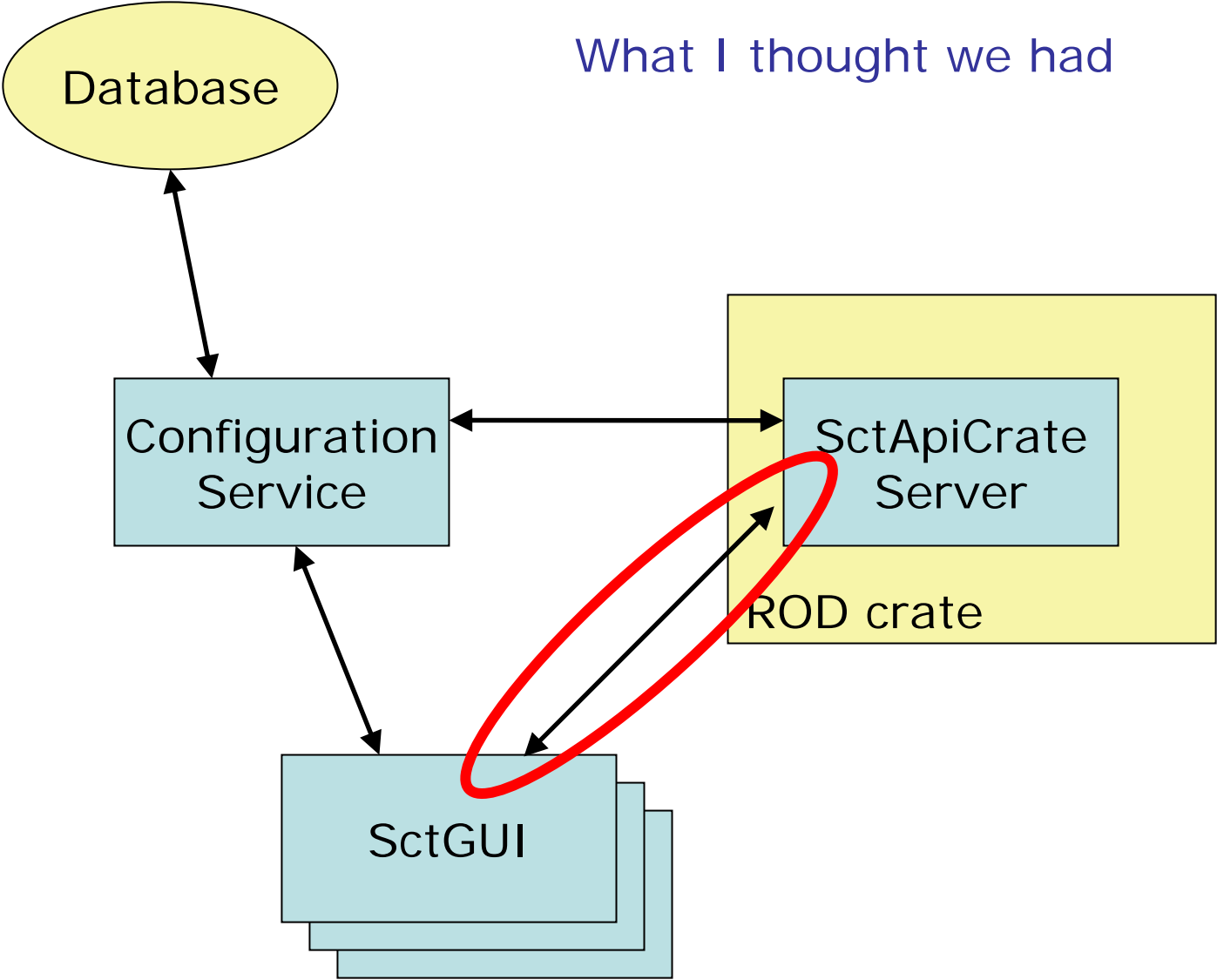


The configuration service

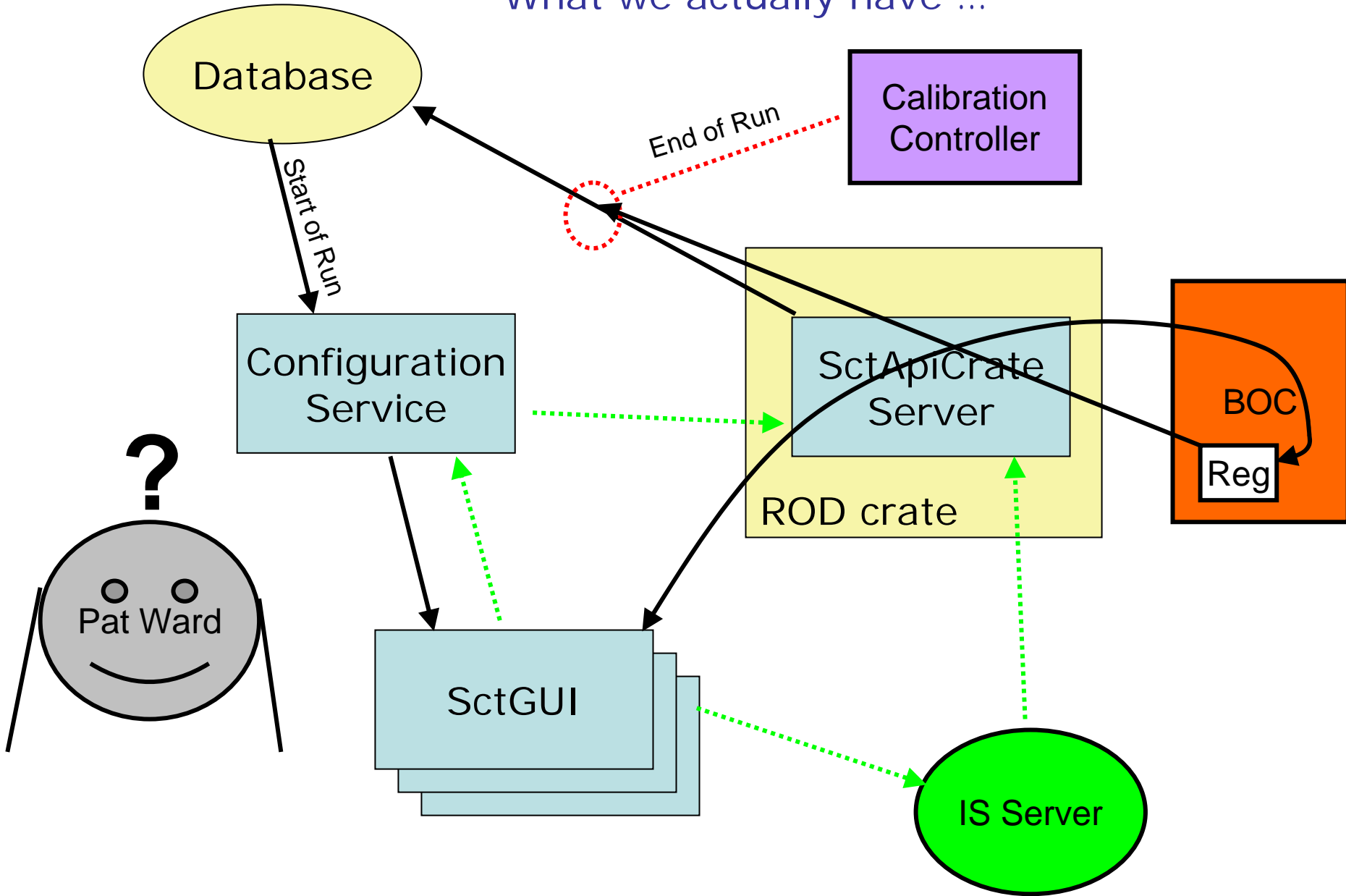
What we might want



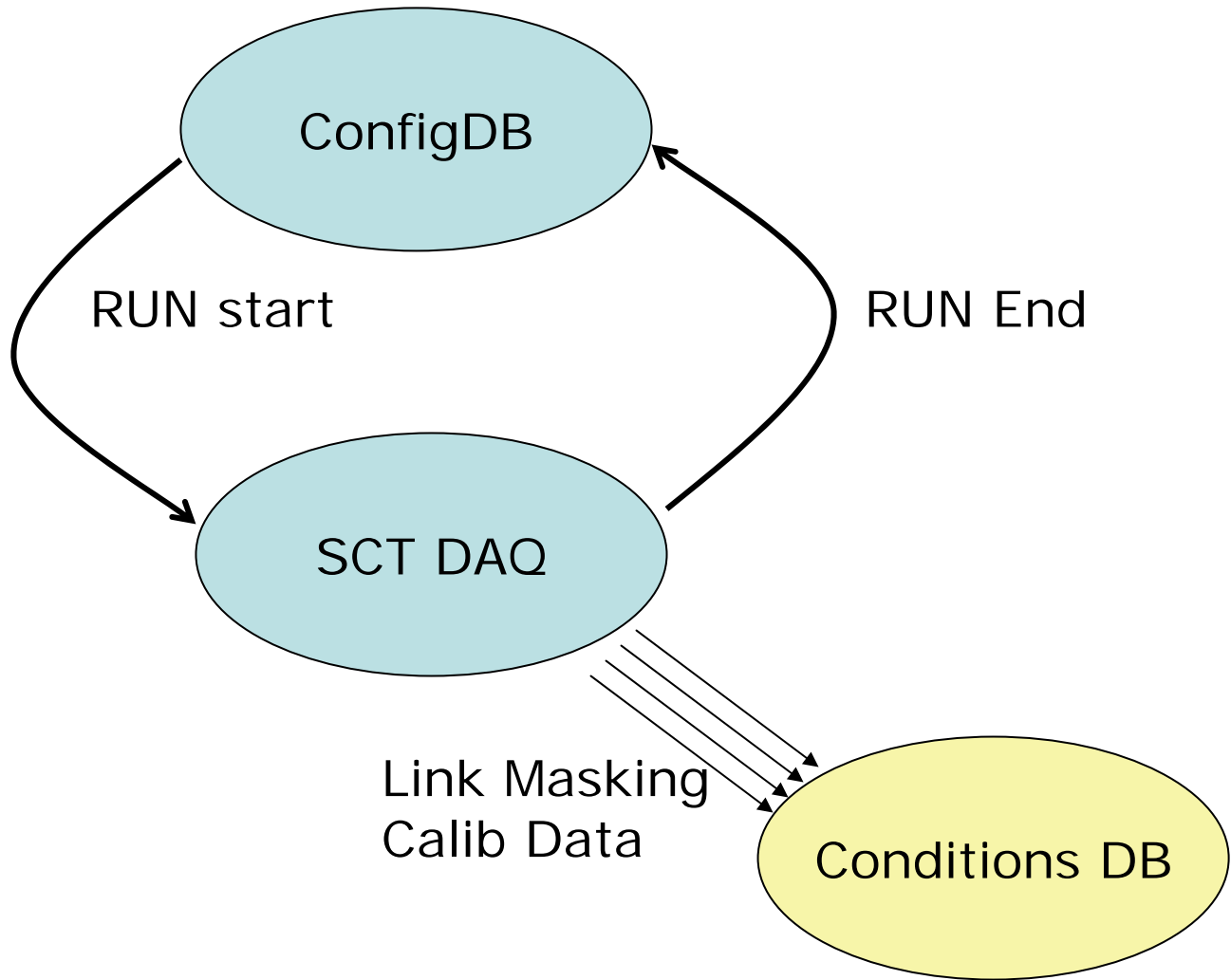
What I thought we had



What we actually have ...



Configuration Database



Configuration Database: Current Situation

