Atlas SCT Off-Detector Electronics: Back-Of-Crate

Maurice Goodrick and Richard Shaw of University of Cambridge

BOC De-Multiplexing of 80MS/s Streams

This note describes the tests done to show the viability of the proposed implementation of the de-multiplexing hardware. It is a progress report rather than an exhaustive account.

1. Introduction

Fibre-Optic cables from some Pixel Silicon modules will carry data at 80MS/s. The ROD accepts data at 40MS/s. For such signals it is planned that the BOC should demultiplex each 80MS/s stream into 2x40MS/s streams. BOC0, the prototype version of BOC, attempts to make provision for this mode of operation for 12x80MS/s streams.

If implemented on BOC1, the pre-production model, up to 48x80MS/s streams could be handled (this would exceed the foreseen modularity of the Pixel project, so BOCs intended for Pixel work would probably be underpopulated).

This note describes work showing that the proposed circuits are delivering the required functionality.

2. Circuits

Three quarters of the BOC0 data streams use dedicated registers to perform the data synchronisation and timing functions required for the SCT strip detector streams. The remaining streams use a CPLD to perform the same functions. These are the streams that offer the 80 to 40 MS/s de-multiplexing. When in this mode, the configuration within the CPLD is as shown in Fig 1. The relative phase of the V- and B-Clocks is adjustable within the BOC clock generation circuits: for this task they are in antiphase.

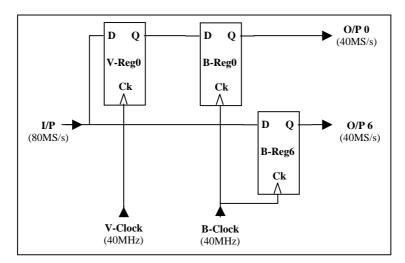


Figure 1: CPLD Configuration for De-Multiplexing

3. Generation of 80MS/s Test Data

The test set-up developed at Cambridge was modified to generate pre-defined 80MS/s data streams. The SLOG was used to generate 2x40MS/s streams. The BOC-Rig front-of-crate module has provisions for merging 2 such data streams into a single stream in electrical form. This is passed to one of the BOC Control streams. The Control stream chosen is one that has been modified to by-pass the BPM chip, so the electrical signal is converted directly into an optical one. The timing of the signals has been trimmed to give a clean 80MS/s optical signal. This is fed-back into the BOC Data stream under test via a short fibre ribbon.

4. The Test Data

The test data is a 64-bit string made by merging 2x32 bit streams from SLOG streams 0 and 6. A number of data patterns have been used, but the ones presented here give the best indication of the performance. Figures 2 and 3 show the make-up of this bit-stream.

5. Capture of De-Multiplexed Data

BOC-Rig can be configured to record the data streams received from BOC in much the same way as a digital scope: the data of each monitored stream is clocked into a long shift register (of up to 120 stages). One of the SLOG front-panel outputs can be used as a trigger. A pre-defined number of clock ticks after the trigger, the shifting stops. The captured data can then be accessed from VME.

6. Observing the Data

The data sequences captured in this way from the two de-multiplexed streams as a function of the data delay that BOC can introduce in each data path before the demultiplexing circuits in the CPLD. This delay is implemented using an ATLAS PHOS4 delay chip, which contains four programmable delays over a range of 25ns in 1ns steps.

7. Interpreting the Data

The data captured on the 2 de-multiplexed streams is shown in Figures 4 and 5. The same data sequence was sent 99 times for each delay setting. The number of times a bit was set for each time slot and each delay was counted, and is shown in the Figures. For visual clarity, the zeros have been replaced by "..". The input data (from the SLOG) is also shown as I/P0 and I/P6 at the head of the Figures. It can be seen that for a range of delay settings the data is correctly recovered: this is shaded GREEN. It can also be seen that for another range of delay settings the data from the wrong stream is recovered, possibly a tick late: this is shaded BLUE. Between these ranges there is a GREY region where the data recovery is unreliable. For stream 0, delays from 5 to 15ns give good data. For stream 6, the good range is from 6 to 16ns. Thus delays in the range 6 to 15ns give good data on both streams.

8. Conclusions

At best the region of good data recovery can only be 12.5 ns wide. In practice, noise and data timing errors will reduce this width. Seeing a working range of 10ns is pleasing. Clearly these tests are not exhaustive: a proper investigation of Bit Error Rate with all streams carrying data is called for. But, given the large margin that has been demonstrated, it is considered safe to use this design for BOC1, the production prototype.

...ooOoo...

This page deliberately left blank

Time (ns) >	0	2	5	5	0 	7	5 	10) 0 	12	25 	15	50 	
SLOG Stream 0 (40MS/s) >		0:0	0 :	:1	0	: 2	0	: 3	0	: 4	0	: 4	0	: 6
SLOG Stream 6 (40MS/s) >		6:0	6 :	:1	6	: 2	6	: 3	6	: 4	6	: 5	6	: 6
Merged Data (80MS/s) >		0:0 6:0	0:1	6:1	0:2	6:2	0:3	6:3	0:4	6:4	0:5	6:5	0:6	6:6

Figure 2: Stream Merging (Notation is <S:B> where <S> is the Stream, is the Bit number in the data sequence)

Stream 0>	1 0 0 0 1 1 1 1 0 0 0 0 1 0 0 0 1 0 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0
Stream 6>	0 0 0 0 0 1 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0
Merged >	100000001010111000000101110100001000100101

Figure 3: The Patterns Used

```
PIX-Mode Data Delay Scan - Double registered in PIX pld
BOC Vernier Clock Control read back as CO hex
Pattern (0x8f088f01) > 8f088f01, Active Streams (0x041) > 41, Events per Delay (100) > 99
HITs for stream 0
      6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
         99 .. .. .. 99 99 99 99
        .. .. .. 99 99 99 99 .. .. ..
                    99 .. .. .. 99 99 99 99
        99 ... ... 99 99 99 99 ... ...
    De1= 9
De1=11
De1=12
De1=13
De1=14
```

Figure 4: Stream 0 De-Multiplexed Data v Data Delay

Patter	n	(0x8	£08	8£0	1)	>	8 f	088	3£0	1,	Ac	ti	ve	st	re	ams	3 (0x(041	.)	> 4	11,	Εv	en	ts	peı	c D	ela	ay	(1	.00) >	9	9										
HITs	for	str	eam	6																																								
ick> 0 P0 > 0 P6 > 0) 1) 0) 0	2 : 1 : 0 :	3 4 0 0 0 0	5 0 0	6 1 0	7 1 0	8 1 1	9 1 1 0	0 1 0 0	1 1 0 0	2 1 0 1	3 1 0	1	5 1 0 1	0	0	8 1 1 0	0	0	0	22 2 1 0	1	4 25 1 1) (0 (31 0 1	32 0 0	33 1 0	34 0 0	35 0 0	0	0	0	0	•	0	2 4 0 0	3 4 0 0	4 4 0 0	5 40 0 0	5 47
1= 6 1= 7 1= 8 1= 9 1=10 1=11 1=13 1=14 1=15 1=16	99 99 99			99 99 4 	99 9 99 9 99 9 99 9 99 9 99 9 99 9 99			1		999999999999	. 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9		9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	999999999999999999999999999999999999999	. 9 9	9	99999	999999999999999999999999999999999999999	999999999999999999999999999999999999999	999999999999999999999999999999999999999	99 99 88 9 8		999999999999999999999999999999999999999	· · · · · · · · · · · · · · · · · · ·		99 99 99 99 99 99 99 99 99 99	97 99 99 99 99 99 99 99 99 1	1 99 99 99 99 99 99 99 99 99 99	99 99 99 99 99 55							999999999999999999999999999999999999999	5 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9							

Figure 5: Stream 6 De-Multiplexed Data v Data Delay

...ooOoo...