TestPI for BOC
05-Jul-04

BOC Board

PHOS4
Clock Delay

TX PlugIn Site

PECL Clock

Received BPM Clock

3v3

CSD[6:0]

LVT

Data [6:0]

HC

CA[5:0]

HCT

Address [5:0]

CBPMWR,CBPMCE

Controls

BPMRST

Reset

Nc7sz08

MDAC Ctls<5>

Laser MDAC Control

BPM Interface

MDAC & BPM
Command Capture

TX CPLD

BOC Test PlugIn
TX Board

XC[11:0]

Module Control Data

LAS_REF_EN

VCC_1 (5v)

5v

3v3 Reg

Local 3v3

Power & Ground
Monitoring

Data Manipulation

GND_2

GND_3

VCC_2 (5v)

GND_1

12 Data Streams
& 1 Status Line

RX Board

nc

RXDAT[11:8]

RXDAT[7:4]

RXDAT[3:0]

4

Note Swap of Streams:
[11:0] <= [0:11]

RX PlugIn
Odd Site

3v3s <5>

GNDs <5>

GND

Power & Ground
Monitoring

MD_ODD_EN

MDDAT,MDCLK,MDCLR

MD_EVEN_EN

Odd Site
Threshold
MDAC Control

VPIN

RX CPLD

BOC Test PlugIn
RX Board

3v3s <4>

GNDs <6>

MD_ODD_EN

MDDAT,MDCLK,MDCLR

MD_EVEN_EN

Even Site
Threshold
MDAC Control

DAC
Control

DAC
Control

Odd_Site_VPIN

VPIN

I_Sink

DAC16

I_Sink

DAC16

3v3 for RX board

RX PlugIn
Even Site

3v3

RXDAT[11:8]

RXDAT[7:4]

RXDAT[3:0]

SLOG

BOC_RIG2

BOC

Xtal Clock

Data Gen

Clock Distribution

Module Control Data

Laser MDAC & BPM Commands

BPM Clock

Laser MDAC & BPM Commands

Module Control Data

Clock Gen

MDAC and BPM Command Capture

Data Manipulation

Test PI TX Board

TX Site 3

TX Site 2

TX Site 1

TX Site 0

Threshold MDAC Settings

Monitor Data

SetUp Bus

BOC Control CPLD

BOC-RIG Control CPLD

PIN Current Monitors

12 Data Streams + 1 Status Line

RX Site 7

RX Site 6

RX Site 5

RX Site 4

RX Site 3

RX Site 2

RX Site 1

RX Site 0

Test PI RX Board

Data Streams

RX CPLD

RX CCT

Select 12 from 96

Data Capture

IPIN

MDAC Re-Format

DAC16

I_Sink

Stream Order Swap:

[11:0] <= [0:11]

Ground & Power Status Monitor

VME

TestPI_SetUp

TestPI_SetUp of 02-Jul-04

Using BOC Test PlugIn with SLOG and BOC-RIG2

Address Offset [3]		Write		Read		Notes
VME	S-Bus	Action	Definition	Action	Definition	
+7E	+3F	MODE	Yet to be defined	MODE	Yet to be defined	
+7C	+3E	CKCTRL	[0,0,0,0,0,PCKD4,PCKINH]	CKCTRL	[0,0,0,0,0,PCKD4,PCKINH]	
+7A	+3D	_		_		
+78	+3C	DEL4	[x,x,D4..D0] 0-24dec	_		
+76	+3B	DEL3	[x,x,D4..D0] 0-24dec	I2CBUSY	[0,0,0,0,0,0,I2C_Busy]	
+74	+3A	DEL2	[x,x,D4..D0] 0-24dec	STATS	[0,0,VCHK1,GCHK2,GCHK1,RXPWRCHK,VREF_EN]	
+72	+39	DEL1	[x,x,D4..D0] 0-24dec	DREG	[D6,D5,D4,D3,D2,D1,D0]	[2]
+70	+38	DEL0	[x,x,D4..D0] 0-24dec	AREG	[RnW,A5,A4,A3,A2,A1,A0] RnW = 1 for Read Op's	[2]
+6E	+37	_		_		
+6C	+36	_		_		
+6A	+35	_		MDHIH	[0,0,MDHi15..MDHi11]	
+68	+34	_		MDHIM	[MDHi10..MDHi4]	
+66	+33	_		MDHIL	[MDHi3..MDHi0,0,0,0]	
+64	+32	_		MDLOH	[0,0,MDLo15..MDLo11]	
+62	+31	_		MDLOM	[MDLo10..MDLo4]	
+60	+30	_		MDLOL	[MDLo3..MDLo0,0,0,0]	
+5E	+2F	_		_		
+5C	+2E	_		_		
+5A	+2D	_		_		
+58	+2C	_		_		
+56	+2B	_		_		
+54	+2A	_		_		
+52	+29	_		_		
+50	+28	_		_		
+4E	+27	_		_		
+4C	+26	_		_		
+4A	+25	_		_		
+48	+24	_		_		
+46	+23	_		_		
+44	+22	_		_		
+42	+21	_		_		
+40	+20	_		_		
+3E	+1F	_		_		
+3C	+1E	_		_		
+3A	+1D	_		_		
+38	+1C	_		_		
+36	+1B	_		_		
+34	+1A	_		_		
+32	+19	_		_		
+30	+18	_		_		
+2E	+17	_		_		
+2C	+16	_		_		
+2A	+15	_		_		
+28	+14	_		_		
+26	+13	_		_		
+24	+12	_		_		
+22	+11	_		_		
+20	+10	_		_		
+1E	+0F	_		_		
+1C	+0E	_		_		
+1A	+0D	_		_		
+18	+0C	_		_		
+16	+0B	_		_		
+14	+0A	_		_		
+12	+09	_		_		
+10	+08	_		_		
+0E	+07	_		_		
+0C	+06	_		_		
+0A	+05	_		_		
+08	+04	_		_		
+06	+03	_		MANUF	= 4B Hex (Add Bit7 to give CB)	
+04	+02	_		MOD_TYPE	= 30 Hex, 48 Dec	
+02	+01	_		REV	= 0	
+00	+00	_		S_No	(0-127; Set in JED file: as on Bar Code Label)	

Load AREG and DREG for both WRITE and READ operations in this Address Range

Notes:

[1] The data path has only [Bit6..Bit0]; Bit7 is ignored on Write, and undefined on Read

[2] Set by last READ or WRITE in Add Range 0-37Hex

[3] Full BOC-RIG VME Address given by: 700000hex + (TXSite * 80hex) + VME Offset or VME Base + VME Offset

700,	
VME Base	SBus Base
700,180	180
700,100	100
700,080	080
700,000	000

The only active communication with the RX Sites is by writing to its Threshold DAC addresses.
This controls a precision current sink which draws current from the RX Site's VPIN supply.
The effect can be monitored by the VPIN Current monitoring circuits of BOC.
This mechanism not only checks out the control paths for the Threshold DACs (of which there are 2 per RX Site),
but also checks and calibrates the monitoring circuits and the VPIN supplies.
The duplicate Ground and 3v3 connections to each site are monitored, and a single Status line for
each pair of RX Sites is passed to its TX Test PlugIn to indicate whether all is OK.