B-Layer Notes:

Pixel Requirements (Provisional):

0) 1 Clock and Control fibre per module

1) 2 Data fibres per module: the data is split into 4-bit nibbles by the MCC: bits 0 and 2 are time multiplexed onto one fibre, and bits 1 and 3 onto the other. The first bit of a data packet always appears as bit 0. Each data fibre carries 80 MBit/s data, giving an aggregate data rate of 160 MBit/s per Pixel module.

2) 6 or 7 modules per BOC/ROD

3) all fibres connect as 8-way ribbons: 1 Clock and Control ribbon, and 2 Data ribbons

BOC and ROD Loading:

0) BOC needs only 1 Opto-TX card loaded in location OTX0

1) ROD needs only serve Clock and Control streams [9:2]

2) BOC has only 2 Opto-RX cards loaded in locations ORX0 and ORX4

3) BOC needs only PHOS4 Data Delay chips for BOC streams [11:0] and [59:48] (i.e. 6 PHOS4s)

4) BOC has only 2 RX-PLDs loaded, RX-PLD0 and RX-PLD2

5) ROD has only 4 Formatters loaded in locations [0,1,4,5]

6) BOC loading may be more than the minimum to simplify spares

Restrictions and *Suggestions*:

0) **The 2 data fibres from one B-Layer module must be an adjacent even-odd pair**

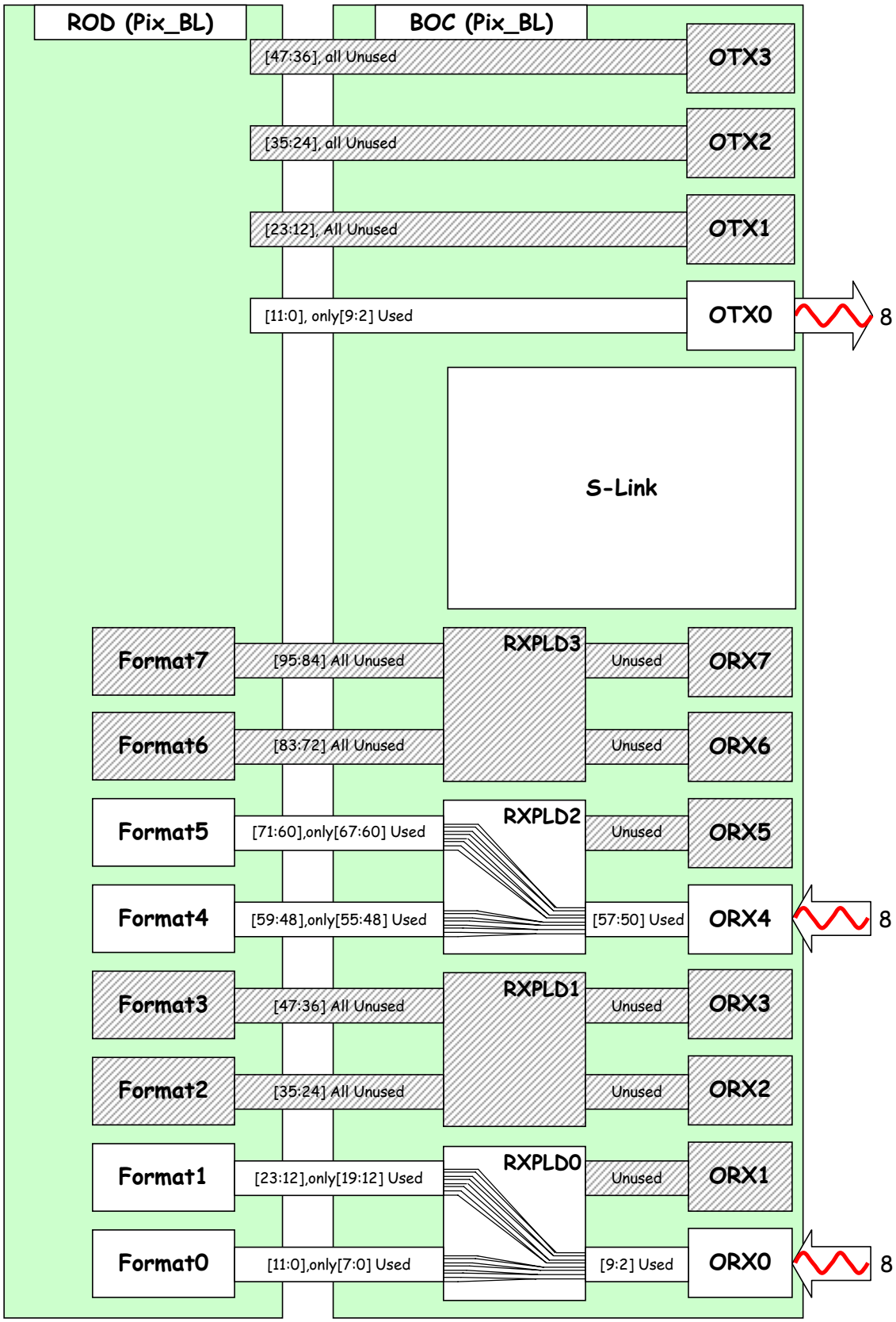
1) **A consistent mapping of data to streams should be maintained**

2) *It is suggested that the first (Even) fibre carries bits 0 and 2, while the second (Odd) fibre carries bits 1 and 3*

3) **Within these restrictions, the ROD burden should be shared reasonably evenly between the loaded formatters.**

4) *A scheme that would suit is: (module 6 is not always present)*

Module	: 0	0	1	1	2	2	3	3	4	4	5	5	6	6
Ribbon	: 0	0	0	0	0	0	0	0	1	1	1	1	1	1
Fibre	: 0	1	2	3	4	5	6	7	0	1	2	3	4	5
BOC S#	: 2	3	4	5	6	7	8	9	50	51	52	53	54	55
ROD S#	: 0,1	2,3	4,5	6,7	12,13	14,15	16,17	18,19	48,49	50,51	52,53	54,55	60,61	62,63
Format#	: 0,0	0,0	0,0	0,0	1,1	1,1	1,1	1,1	4,4	4,4	4,4	4,4	5,5	5,5



Layers B Layer

PROVISIONAL

B-Layer Mapping (first half)

ROD		BOC					Pixel Data Stream			
ROD Formatter	ROD I/P Stream	Threshold DAC #	Data Delay #	Data CPLD #	RX Stream #	OptoRX <#:Stream>	First/Second	Fibre Number	Fibre Ribbon	Module #
0	0	2	2	0	2	0:2	F	0	0	0
	1						S			
	2	3	3		3	0:3	F	1		
	3						S			
	4	4	4		4	0:4	F	2		1
	5						S			
	6	5	5		5	0:5	F	3		
	7						S			
	8									
	9									
	10									
	11									
1	12	6	6		6	0:6	F	4	0	2
	13						S			
	14	7	7		7	0:7	F	5		
	15						S			
	16	8	8		8	0:8	F	6		3
	17						S			
	18	9	9		9	0:9	F	7		
	19						S			
	20									
	21									
	22									
	23									
2	24			1						
	25									
	26									
	27									
	28									
	29									
	30									
	31									
	32									
	33									
	34									
	35									
3	36									
	37									
	38									
	39									
	40									
	41									
	42									
	43									
	44									
	45									
	46									
	47									

Layers B Layer

PROVISIONAL

B-Layer Mapping (2nd part)

ROD		BOC					Pixel Data Stream			
ROD Formatter	ROD I/P Stream	Threshold DAC #	Data Delay #	Data CPLD #	RX Stream #	OptoRX <#:Stream>	First/Second	Fibre Number	Fibre Ribbon	Module #
4	48	50	50	2	50	4:2	F	0	1	4
	49						S			
	50	51	51		51	4:3	F	1		
	51						S			
	52	52	52		52	4:4	F	2		5
	53						S			
	54	53	53		53	4:5	F	3		
	55						S			
	56									
	57									
	58									
	59									
5	60	54	54		54	4:6	F	4	1	6
	61						S			
	62	55	55		55	4:7	F	5		
	63						S			
	64	56	56		56	4:8	F	6		7
	65						S			
	66	57	57		57	4:9	F	7		
	67						S			
	68									
	69									
	70									
	71									
6	72			3						
	73									
	74									
	75									
	76									
	77									
	78									
	79									
	80									
	81									
	82									
	83									
7	84									
	85									
	86									
	87									
	88									
	89									
	90									
	91									
	92									
	93									
	94									
	95									

Layer 1 Notes:

Pixel Requirements (Provisional):

0) 1 Clock and Control fibre per module

1) 1 Data fibre per module: even and odd data bits are time multiplexed onto the one fibre, giving a data rate of 80 MBit/s per Pixel module.

2) 13 modules per BOC/ROD

3) all fibres connect as 8-way ribbons: 2 Clock and Control ribbons, and 2 Data ribbons

BOC and ROD Loading:

0) BOC needs only 2 Opto-TX cards loaded in locations OTX0 and OTX1 (?? or 0 & 2 ??)

1) ROD needs only serve Clock and Control streams [9:2] and [21:14] (?? or [9:2] & [33:26] ??)

2) BOC has only 2 Opto-RX cards loaded in locations ORX0 and ORX4

3) BOC needs only PHOS4 Data Delay chips for BOC streams [11:0] and [59:48] (i.e. 6 PHOS4s)

4) BOC has only 2 RX-PLDs loaded, RX-PLD0 and RX-PLD2

5) ROD has only 4 Formatters loaded in locations [0,1,4,5]

6) BOC loading may be more than the minimum to simplify spares

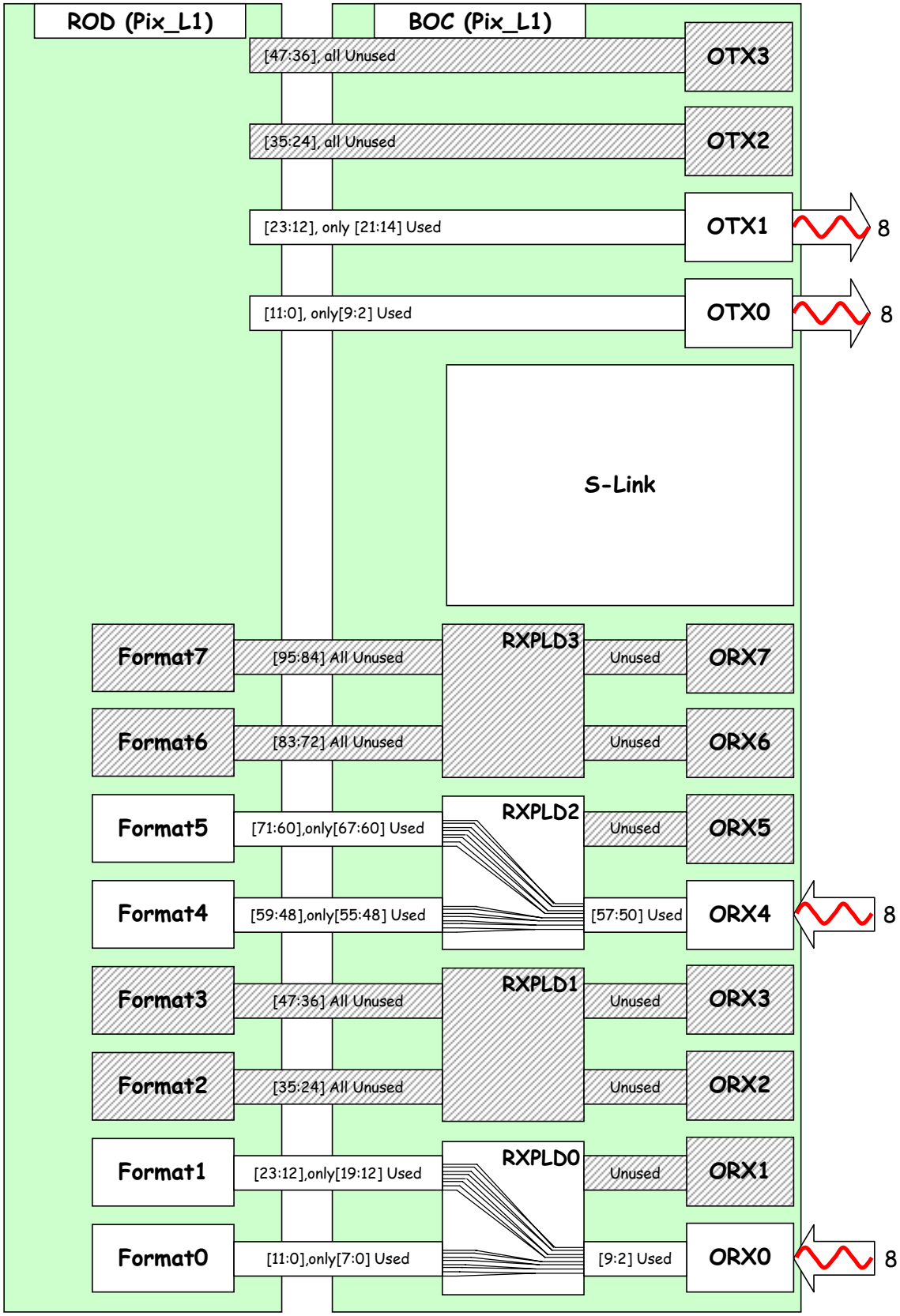
Restrictions and *Suggestions*:

0) A consistent mapping of data to streams should be maintained

1) **Within these restrictions, the ROD burden should be shared reasonably evenly between the loaded formatters.**

2) *A scheme that would suit is:*

Module	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*
Ribbon	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*	*1*	*1*
Fibre	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*0*	*1*	*2*	*3*	*4*
BOC S#	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*50*	*51*	*52*	*53*	*54*
ROD S#	*0,1*	*2,3*	*4,5*	*6,7*	*12,13*	*14,15*	*16,17*	*18,19*	*48,49*	*50,51*	*52,53*	*54,55*	*60,61*
Format#	*0,0*	*0,0*	*0,0*	*0,0*	*1,1*	*1,1*	*1,1*	*1,1*	*4,4*	*4,4*	*4,4*	*4,4*	*5,5*



Layers Layer 1

PROVISIONAL

Layer 1 Mapping (first half)

ROD		BOC					Pixel Data Stream		
ROD Formatter	ROD I/P Stream	Threshold DAC #	Data Delay #	Data CPLD #	RX Stream #	OptoRX <#:Stream>	First/Second	Fibre Number	Fibre Ribbon
0	0	2	2	0	2	0:2	F	0	0
	1						S		
	2	3	3		3	0:3	F	1	
	3						S		
	4	4	4		4	0:4	F	2	
	5						S		
	6	5	5		5	0:5	F	3	
	7						S		
	8								
	9								
	10								
	11								
1	12	6	6		6	0:6	F	4	0
	13						S		
	14	7	7		7	0:7	F	5	
	15						S		
	16	8	8		8	0:8	F	6	
	17						S		
	18	9	9		9	0:9	F	7	
	19						S		
	20								
	21								
	22								
	23								
2	24			1					
	25								
	26								
	27								
	28								
	29								
	30								
	31								
	32								
	33								
	34								
	35								
3	36								
	37								
	38								
	39								
	40								
	41								
	42								
	43								
	44								
	45								
	46								
	47								

Layer 1 Mapping (2nd part)

ROD		BOC					Pixel Data Stream		
ROD Formatter	ROD I/P Stream	Threshold DAC #	Data Delay #	Data CPLD #	RX Stream #	OptoRX <#:Stream>	First/Second	Fibre Number	Fibre Ribbon
4	48	50	50	2	50	4:2	F	0	1
	49						S		
	50	51	51		51	4:3	F	1	
	51						S		
	52	52	52		52	4:4	F	2	
	53						S		
	54	53	53		53	4:5	F	3	
	55						S		
	56								
	57								
	58								
	59								
5	60	54	54		54	4:6	F	4	1
	61						S		
	62	55	55		55	4:7	F	5	
	63						S		
	64	56	56		56	4:8	F	6	
	65						S		
	66	57	57		57	4:9	F	7	
	67						S		
	68								
	69								
	70								
	71								
6	72			3					
	73								
	74								
	75								
	76								
	77								
	78								
	79								
	80								
	81								
	82								
	83								
7	84								
	85								
	86								
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	88								
	89								
	90								
	91								
	92								
	93								
	94								
	95								

Layer 2 and Disk Notes:

Pixel Requirements (Provisional):

0) 1 Clock and Control fibre per module

1) 1 Data fibre per module with a data rate of 40 MBit/s

2) 26 modules per BOC/ROD

3) all fibres connect as 8-way ribbons: 4 Clock and Control ribbons, and 4 Data ribbons

BOC and ROD Loading:

0) BOC needs all 4 Opto-TX cards loaded

1) ROD needs only serve Clock and Control streams [9:2], [21:14],[33:26], and [45:38]

2) BOC has only 4 Opto-RX cards loaded in locations ORX0,ORX1,ORX4 and ORX5

3) BOC needs only PHOS4 Data Delay chips for BOC streams [23:0] and [71:48] (i.e. 12 PHOS4s)

4) BOC has only 2 RX-PLDs loaded, RX-PLD0 and RX-PLD2

5) ROD has only 4 Formatters loaded in locations [0,1,4,5]

6) All Pixel BOCs may be loaded to this level to simplify spares

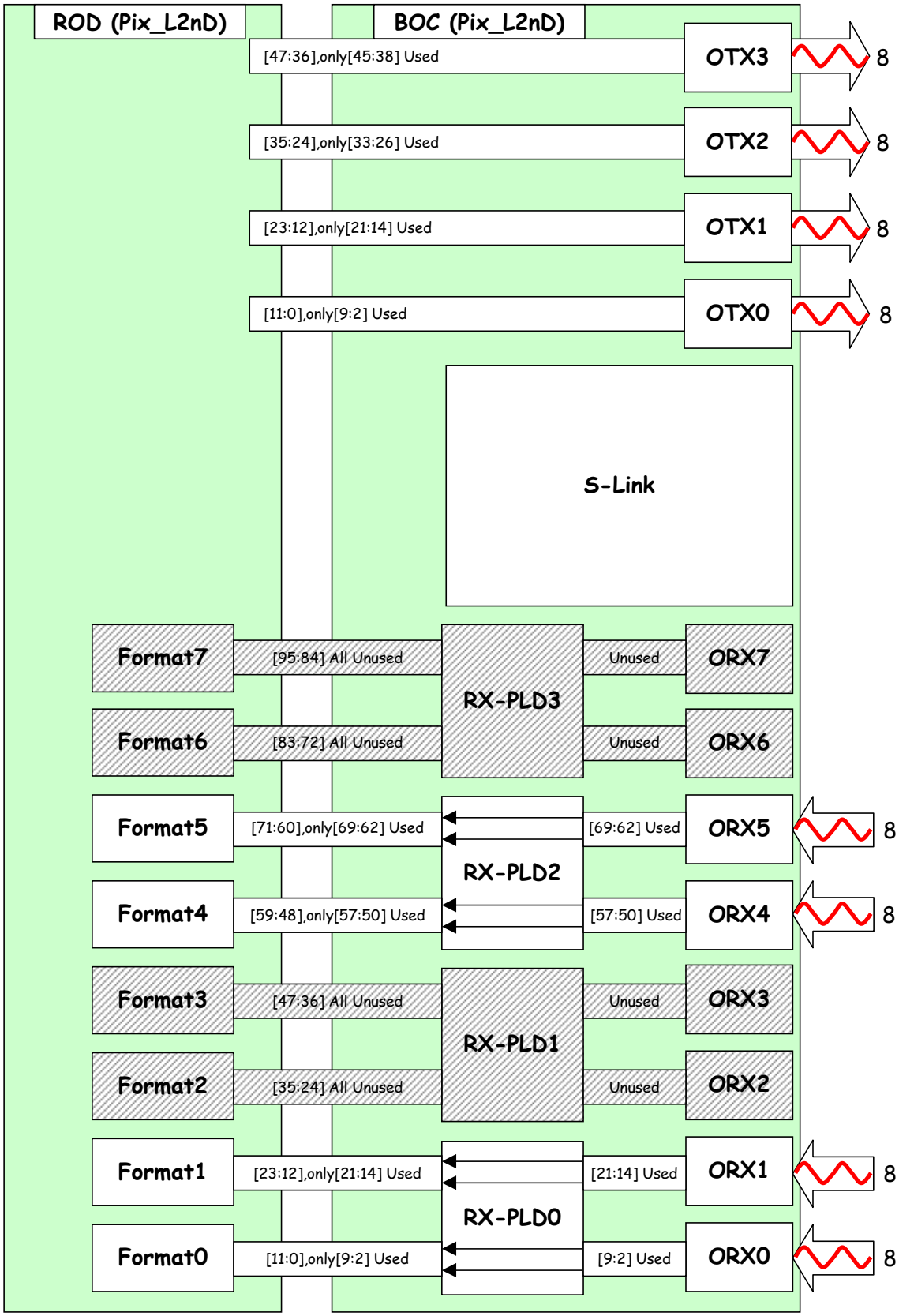
Restrictions and *Suggestions*:

0) A consistent mapping of data to streams should be maintained

1) **Within these restrictions, the ROD burden should be shared reasonably evenly between the loaded formatters.**

2) *A scheme that would suit is:*

Module	:	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	*21*	*22*	*23*	*24*	*25*
Ribbon	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*2*	*2*	*2*	*2*	*2*	*2*	*2*	*3*	*3*	*3*	*3*	*3*
Fibre	:	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*0*	*1*	*2*	*3*	*4*
BOC S#	:	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*50*	*51*	*52*	*53*	*54*	*55*	*56*	*62*	*63*	*64*	*65*	*66*
ROD S#	:	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*50*	*51*	*52*	*53*	*54*	*55*	*56*	*62*	*63*	*64*	*65*	*66*
Format#	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*4*	*4*	*4*	*4*	*4*	*4*	*4*	*5*	*5*	*5*	*5*	*5*


ROD (Pix_L2nD)
BOC (Pix_L2nD)
[47:36],only[45:38] Used
OTX3
8
[35:24],only[33:26] Used
OTX2
8
[23:12],only[21:14] Used
OTX1
8
[11:0],only[9:2] Used
OTX0
8
S-Link
Format7
[95:84] All Unused
RX-PLD3
Unused
ORX7
Format6
[83:72] All Unused
Unused
ORX6
Format5
[71:60],only[69:62] Used
RX-PLD2
[69:62] Used
ORX5
8
Format4
[59:48],only[57:50] Used
[57:50] Used
ORX4
8
Format3
[47:36] All Unused
RX-PLD1
Unused
ORX3
Format2
[35:24] All Unused
Unused
ORX2
Format1
[23:12],only[21:14] Used
RX-PLD0
[21:14] Used
ORX1
8
Format0
[11:0],only[9:2] Used
[9:2] Used
ORX0
8

Layer 2 and Disk Mapping (first half)

ROD		BOC					Pixel Data Stream	
ROD Formatter	ROD I/P Stream	Threshold DAC #	Data Delay #	Data CPLD #	RX Stream #	OptoRX <#:Stream>	Fibre Number	Fibre Ribbon
0	0			0				
	1							
	2	2	2		2	0:2	0	0
	3	3	3		3	0:3	1	
	4	4	4		4	0:4	2	
	5	5	5		5	0:5	3	
	6	6	6		6	0:6	4	
	7	7	7		7	0:7	5	
	8	8	8		8	0:8	6	
	9	9	9		9	0:9	7	
	10							
	11							
1	12							
	13							
	14	14	14		14	1:2	0	1
	15	15	15		15	1:3	1	
	16	16	16		16	1:4	2	
	17	17	17		17	1:5	3	
	18	18	18		18	1:6	4	
	19	19	19		19	1:7	5	
	20	20	20		20	1:8	6	
	21	21	21		21	1:9	7	
	22							
	23							
2	24			1				
	25							
	26							
	27							
	28							
	29							
	30							
	31							
	32							
	33							
	34							
	35							
3	36							
	37							
	38							
	39							
	40							
	41							
	42							
	43							
	44							
	45							
	46							
	47							

Layer 2 and Disk Mapping (2nd half)

ROD		BOC					Pixel Data Stream	
ROD Formatter	ROD I/P Stream	Threshold DAC #	Data Delay #	Data CPLD #	RX Stream #	OptoRX <#:Stream>	Fibre Number	Fibre Ribbon
	48							
	49							
	50	50	50		50	4:2	0	
	51	51	51		51	4:3	1	
	52	52	52		52	4:4	2	
4	53	53	53		53	4:5	3	2
	54	54	54		54	4:6	4	
	55	55	55		55	4:7	5	
	56	56	56		56	4:8	6	
	57	57	57		57	4:9	7	
	58							
	59			2				
	60							
	61							
	62	62	62		62	5:2	0	
	63	63	63		63	5:3	1	
	64	64	64		64	5:4	2	
5	65	65	65		65	5:5	3	3
	66	66	66		66	5:6	4	
	67	67	67		67	5:7	5	
	68	68	68		68	5:8	6	
	69	69	69		69	5:9	7	
	70							
	71							
	72							
	73							
	74							
	75							
	76							
6	77							
	78							
	79							
	80							
	81							
	82							
	83			3				
	84							
	85							
	86							
	87							
	88							
7	89							
	90							
	91							
	92							
	93							
	94							
	95							