

Atlas SCT Off-Detector Electronics: Back-Of-Crate

BOC Timing Functions

This note discusses timing functions to be carried out on the Back-Of-Crate card and how they might be achieved. The implications for ROD functionality are outlined.

1. Requirements

1.1. The Clock and Control Path

- 1.1.1. The Beam Crossing Clock, BX, is received from the TIM module via the backplane. It is planned that this be a copy shared by the ROD and BOC cards residing at this crate slot, with the termination being on the ROD.
- 1.1.2. Four control signals are generated on the ROD, one of which requests a Level 1 Trigger (L1T) to be sent down all (activated?) clock and control streams.
- 1.1.3. Any addition to the L1T latency should be minimised.
- 1.1.4. The Bi-Phase-Mark ASIC (BPM) allows the encoded clock and control signal to be finely delayed over a wide range on a stream-by-stream basis. This is part of the mechanism for detector module timing adjustment, which allows synchronisation of the time quantisation of the front-end electronics with the beam crossings: presumably with an allowance for the times-of-flight of the differently located detector modules.

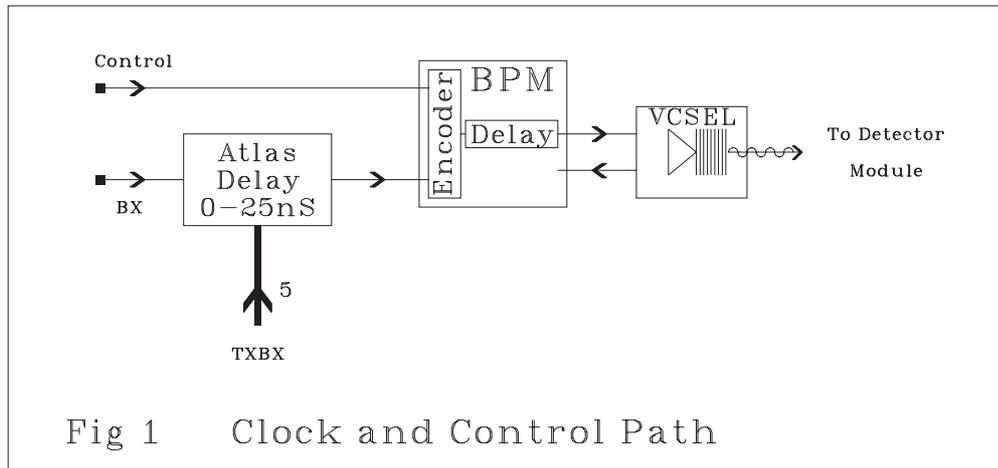
1.2. The Data Path

- 1.2.1. Normal data comprises packets that may arrive asynchronously on the different streams. The timing of the stream data relative to the local clock is random, but will probably be stable over long periods. The BOC must retime this data to be in synchronisation over all the streams, and acceptable to the ROD. The exact time for the data packets to pass through the BOC is not critical, as the ROD is data driven.
- 1.2.2. The detector module synchronisation operation must be supported by the BOC. This operation involves setting the modules into a mode where they first feedback their local clock signal, and then that of the neighbouring module. Note that, in both cases, the 40MHz clock is divided by two before being fed back – presumably to match the bandwidth of the data path. BOC must provide means of comparing the timings of these two fed-back signals with a resolution of around 100pS.
- 1.2.3. There is the possibility that this procedure will not ensure that a particular L1T signal will get all front-ends to sample the same time-bucket: there could be discrepancies of integral numbers of 50nS periods. But this would imply fibre length variations of at least 10m (giving a 50nS variation in L1T arrival time), so this problem should be relatively easy to avoid.

2. Possible Architectural Implementations

2.1. Clock and Control Path

2.1.1. A proposed clock and control path is shown in Fig 1. Four control signals are generated on the ROD, one of which requests a Level 1 Trigger (L1T) to be sent down all (activated?) clock and control streams.

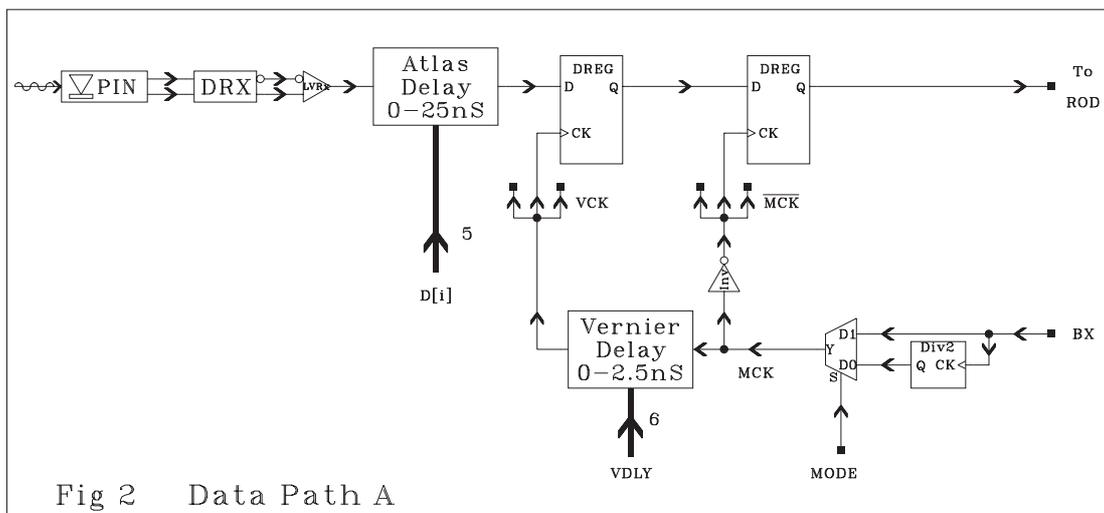


2.1.2. The BX signal has a phase trim of 0-25nS in 1nS steps to allow the BPM to strobe the control signals as soon as they are reliably valid, thus minimising the L1T latency.

2.1.3. The BPM ASIC has two post-encoding delay mechanisms: one allows several steps of 25nS, the other is a fine control of limited range (for details, see BPM spec).

2.2. Data Path A

2.2.1. This is the first of two proposed data paths, and is shown in Fig 2.



2.2.2. For each data stream the PIN diode is closely coupled to a stream of the DRX receiver chip. Its LVDS output is converted to TTL, and is then delayed by up to 25nS in 1nS steps. The delayed output is clocked into a register using a common clock VCK. The

data is clocked into a further register on the falling edge of BX before being passed to the ROD.

- 2.2.3. The delay is determined on a stream-by-stream basis by a 5-bit control words $D[i]$ having values in the range 0 to 24.
- 2.2.4. When in **Data Taking** mode, the MODE control signal is used to select the 40MHz BX clock as the input to the Vernier Delay circuit; this ECLinPS chip gives a vernier delay in the range 0-2.5nS in 40pS steps, controlled by a 6-bit control word VDLY. When in **Timing Trim** mode, the BX clock is divided by two before being fed to the Vernier Delay (to match the 20MHz fed-back clock).

2.3. Data Path B

2.3.1. This is the proposed alternative data path, and is shown in Fig 3.

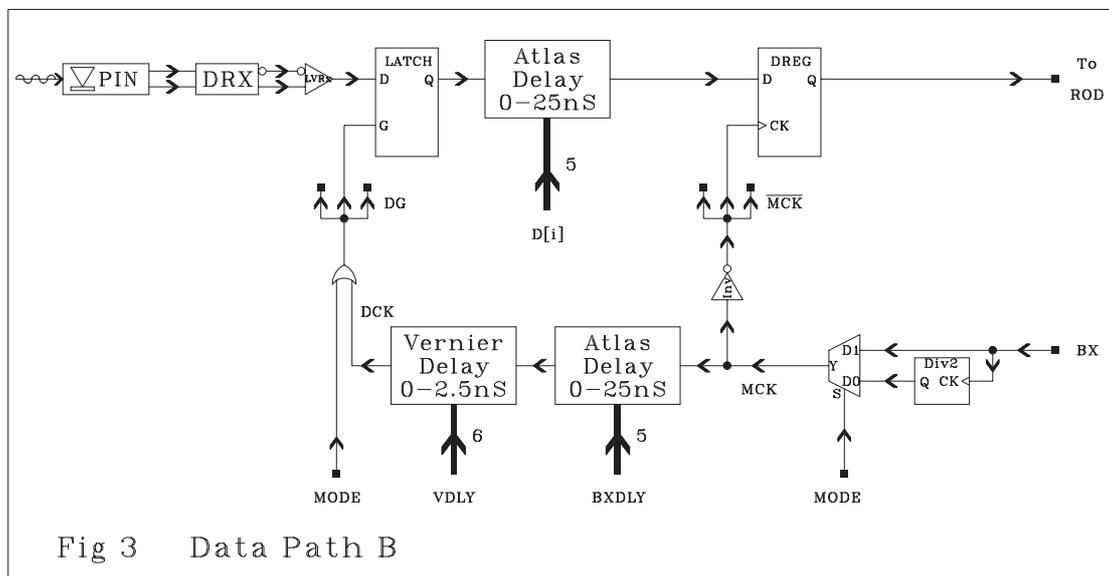


Fig 3 Data Path B

- 2.3.2. The data paths are the same up to the output of the LVDS to TTL converter. This time, the data is fed to a transparent latch. Its output is fed through a 0-25nS delay, and then strobed into a register on the falling edge of MCK before being fed to ROD.
- 2.3.3. The transparent latch is controlled by a gate signal DG: this can either be held high to give transparent operation (for normal data taking), or driven by a common delayed clock DCK that has both coarse (0-25nS), and fine (0-2.5nS) adjustment. The coarse adjustment is determined by a 5-bit control word BXDLY, valued 0-24. The fine control by a 6-bit word, VDLY. The input to this delay chain is MCK, selected as either the 40MHz BX clock, or half that when in **Timing Trim** mode.

3. Outline Procedures

3.1. Using Data Path A for Timing Trim

- 3.1.1. The modules are set to feedback their local clock (divided by two).
- 3.1.2. The vernier delay VDLY is set to mid range, and MODE is set to use the 20MHz clock.

- 3.1.3. $D[i]$ for all streams is set to 0, and ROD set to record the proportion of 1's and 0's seen on each stream. Note that this is no package structure to the signal arriving on each stream; the ROD should just make multiple samples of the state of the data.
- 3.1.4. This is repeated for $D[i]$ 1 to 24.
- 3.1.5. The phase of the received clocks should be recoverable from the recorded data to better than 1nS.
- 3.1.6. The modules are then instructed to feedback the neighbouring clock (halved).
- 3.1.7. The phase measurement is repeated for this signal.
- 3.1.8. The required adjustments can now be made to the BPM delays.
- 3.1.9. A further iteration can now be made, this time also making use of the vernier delays to give a finer resolution.

3.2. Setting Up Data Path A for Data Taking

- 3.2.1. The modules are set to generate packets of test data.
- 3.2.2. The vernier delay VDLY is fixed (mid range would be fine), and MODE is set to use the 40MHz clock.
- 3.2.3. The delays $D[i]$ are all set to 0, and N data packets are read (N might be of order 1000). The number of damaged packets is recorded for this value of delay for each stream.
- 3.2.4. This operation is repeated for delays 1 to 24.
- 3.2.5. Hopefully there will not only be a clear peak in the number of damaged packets, but there will be a large range of delays without damaged packets.
- 3.2.6. The delay for each stream is then set to as far away from the worst value as possible: i.e. 12.5nS (modulo 25) later.
- 3.2.7. This procedure has found to be effective when using the Atlas Mustard data acquisition module.

3.3. Using Data Path B for Timing Trim

- 3.3.1. Data path B was posited to try get at the fed-back clock signals before they have been degraded by passing through the delay chip. The idea is to make the phase measurement by strobing the signal directly into a latch. Unfortunately it may not avoid the problem, because it necessitates generating a gate whose timing can be swept through the full 25nS in steps of 40pS. The generation of this gate would make use the same 25nS delay chip, so there may be no advantage. But at least the process is only done once. The procedure is very similar to that for Path A.
- 3.3.2. The modules are set to feedback their local clock (halved).
- 3.3.3. The vernier delay VDLY is set to mid range, and MODE is set to use the 20MHz clock.
- 3.3.4. BXDLY is set to 0, and ROD set to record the proportion of 1's and 0's seen on each stream.
- 3.3.5. This is repeated for BXDLY 1 to 24.
- 3.3.6. The phase of the received clocks should be recoverable from the recorded data to better than 1nS.
- 3.3.7. The modules are then instructed to feedback the neighbouring clock (halved).
- 3.3.8. The phase measurement is repeated for this signal.

- 3.3.9. The required adjustments can now be made to the BPM delays.
- 3.3.10. A further iteration can now be made, this time also making use of the vernier delays to give a finer resolution.

3.4. Setting Up Data Path B for Data Taking

- 3.4.1. The MODE control signal is set high, thus holding the Latch in its transparent state.
- 3.4.2. The modules are set to generate packets of test data, and MODE is set to use the 40MHz clock for clocking the D-type register.
- 3.4.3. The delays $D[i]$ are all set to 0, and N data packets are read (N might be of order 1000). The number of damaged packets is recorded for this value of delay for each stream.
- 3.4.4. This operation is repeated for delays 1 to 24.
- 3.4.5. Hopefully there will not only be a clear peak in the number of damaged packets, but there will be a large range of delays without damaged packets.
- 3.4.6. The delay for each stream is then set to as far away from the worst value as possible: i.e. $12.5nS \pmod{25}$ later.

4. ROD Implications

4.1. Timing Adjustment for Normal Data Taking

- 4.1.1. The SetUp bus would be used extensively during these operations
- 4.1.2. The operation could be driven by an off-ROD processor via VME.
- 4.1.3. Timing adjustment would benefit greatly from on-ROD histogramming of packet errors.

4.2. Timing Trim Operation

- 4.2.1. The SetUp bus would be used extensively during these operations
- 4.2.2. The operation could be driven by an off-ROD processor via VME.
- 4.2.3. Timing trim operation would be greatly benefit from on-ROD histogramming of 1's and 0's on a stream-by-stream basis.

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