BOC Laser Interlock

Change Record		
Date	**by**	**Change**
12-May-2000	MJG	Created
15-May-2000	MJG	Status section added. Status section added. Laser Safety referred to ATLAS page. HTML version created.

Status:

The features described in this document are at a preliminary stage; discussion and development are required to arrive at the final design.

Introduction:

The power output by the VCSELs both on the BOC and the detector modules is a potential eye hazard. Interlock features are incorporated in the design of BOC to support safe operation of the system as installed in Atlas. These features will also support safe operation of test and prototype installations.

It is not within the scope of this note to attempt a proper assessment of the laser hazard in the sub-detector. This note is concerned with the provisions for safe working at the rear of the Readout rack.

The document “Laser Safety and ATLAS FE-Links” can be found at:
http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/links/install/laser_safety/

Outline:

Two sources of potentially damaging radiation exist: the lasers on the BOCs which are used to send control signals to the detector modules, and the lasers on the modules themselves, which are used to send the data back to the BOCs.

Although the output from the BOC lasers is higher power, it should be easier to guard against it: an **Access Gate** is provided on the BOCs that is locally interlocked to the on-board lasers. When the gate is shut, laser light from unconnected lasers cannot escape. When open, the lasers are un-powered.

The output of the on-detector lasers is a problem when in groups of 12; so the light that spills from the end of an un-connected fibre ribbon at the crate end could be a hazard. It is hard to see how the connection status of each fibre could be detected and communicated to ***the appropriate*** detector module. What is being provided should inhibit all the on-detector lasers when work is being carried out at the back of the

rack. It is also foreseen that exceptional circumstances may arise when such an interlock needs to be defeated, and a key-operated override is provided so this can be achieved in a controlled manner. Clearly safety will depend crucially on good working procedures being followed, especially when the interlock is overridden.

Description:

Figure 1 shows the interlock circuitry on the BOCs and how it interacts with the Laser-Interlock line on the crate backplane. The **Opto Access Gate** must be opened to insert or remove either command or data fibre connectors. There are two microswitches that are operated when the gate is opened: if either is operated, then the local laser inhibit signal is asserted, and a common Laser-Interlock line running along the P3 backplane of the crate is pulled down. The state of the two signals (the local and the external) is displayed by two LEDs labeled **INT** and **EXT** at the rear of each BOC, and may be accessed as two bits in a Status Word that can be read via the Setup Bus and the corresponding ROD. Note that an open gate on any BOC will lead to all the **EXT** LEDs to light, but only the one **INT** LED.

The Laser-Interlock signal is bussed to the end of the backplane, where it is connected to one pin of a 3-pin connector: the other pins provide access to +5 volt power. This is the route to apply the interlock to the LV power supply that feeds the on-detector lasers. As the mapping of modules to fibres is complicated, it will probably be necessary to inhibit the lasers of all the Silicon detector modules if any one **Opto Access Gate** is open.

Figure 2 shows how the interlock scheme might be arranged at the rack level. The interlock signals from each crate are brought together in an **Interlock Control Box** (this is shown much larger than it needs to be). This box not only ORs together the signals before passing them on to the module LV PSU, but provides a key-operated override for the interlock. Prototype and laboratory work may use far smaller arrangements: the interlock structure described here should be readily adapted to such systems.

General Notes and References:

1. The backplane information can be found at : http://www.hep.phy.cam.ac.uk/~goodrick/AtBOC/BPlane_and_Slots-MJG.pdf

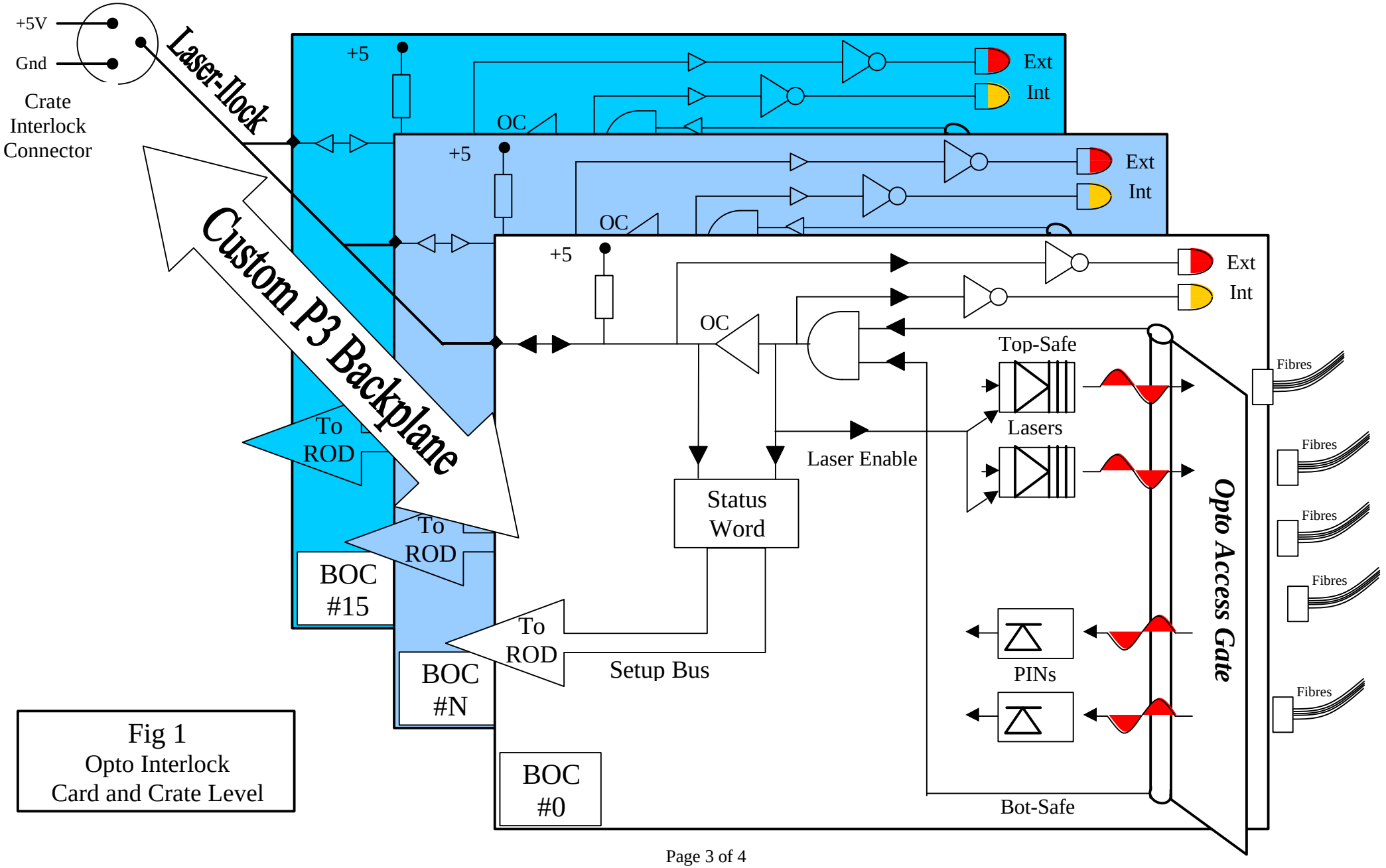

Fig 1
Opto Interlock
Card and Crate Level

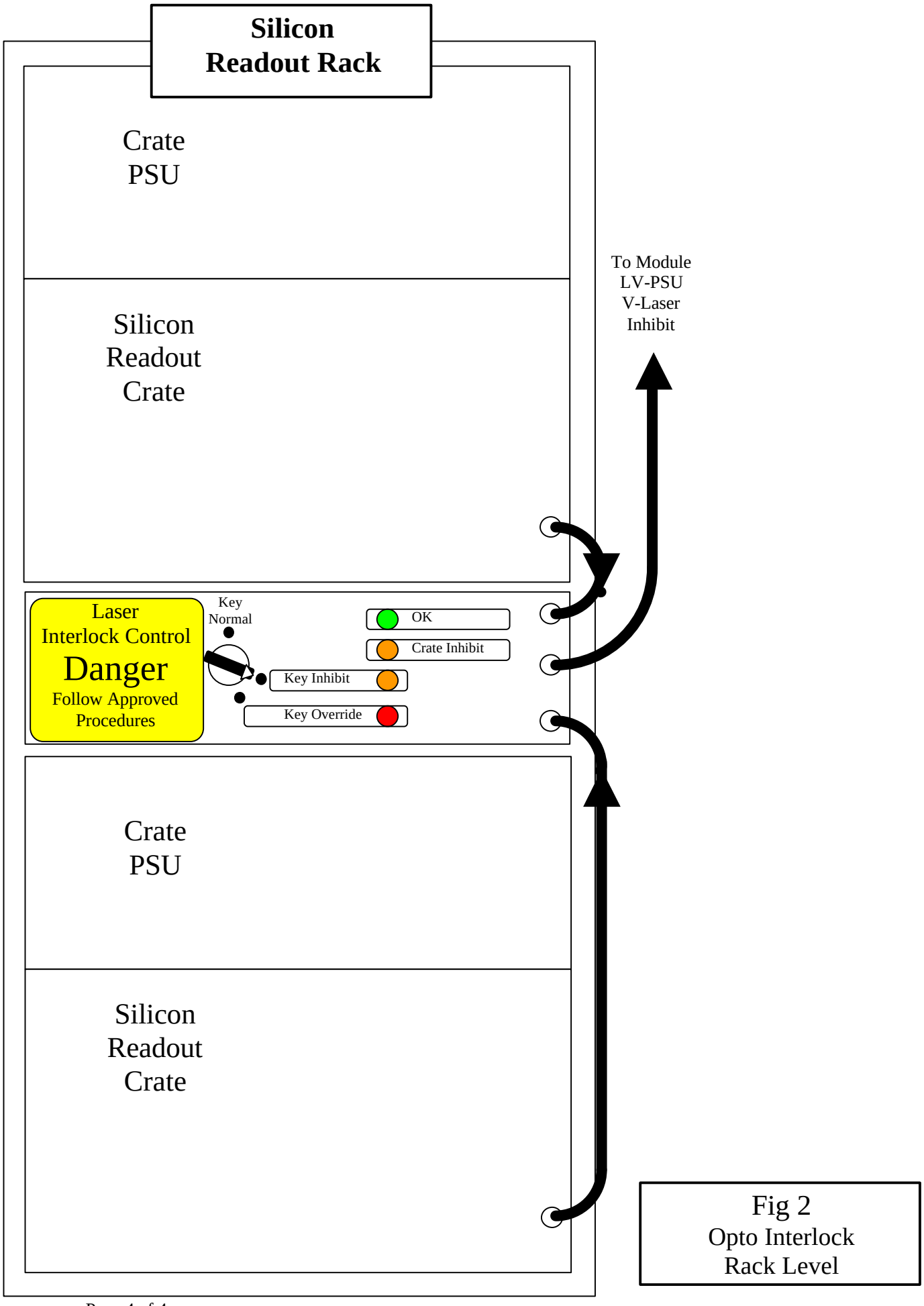

Fig 2
Opto Interlock
Rack Level