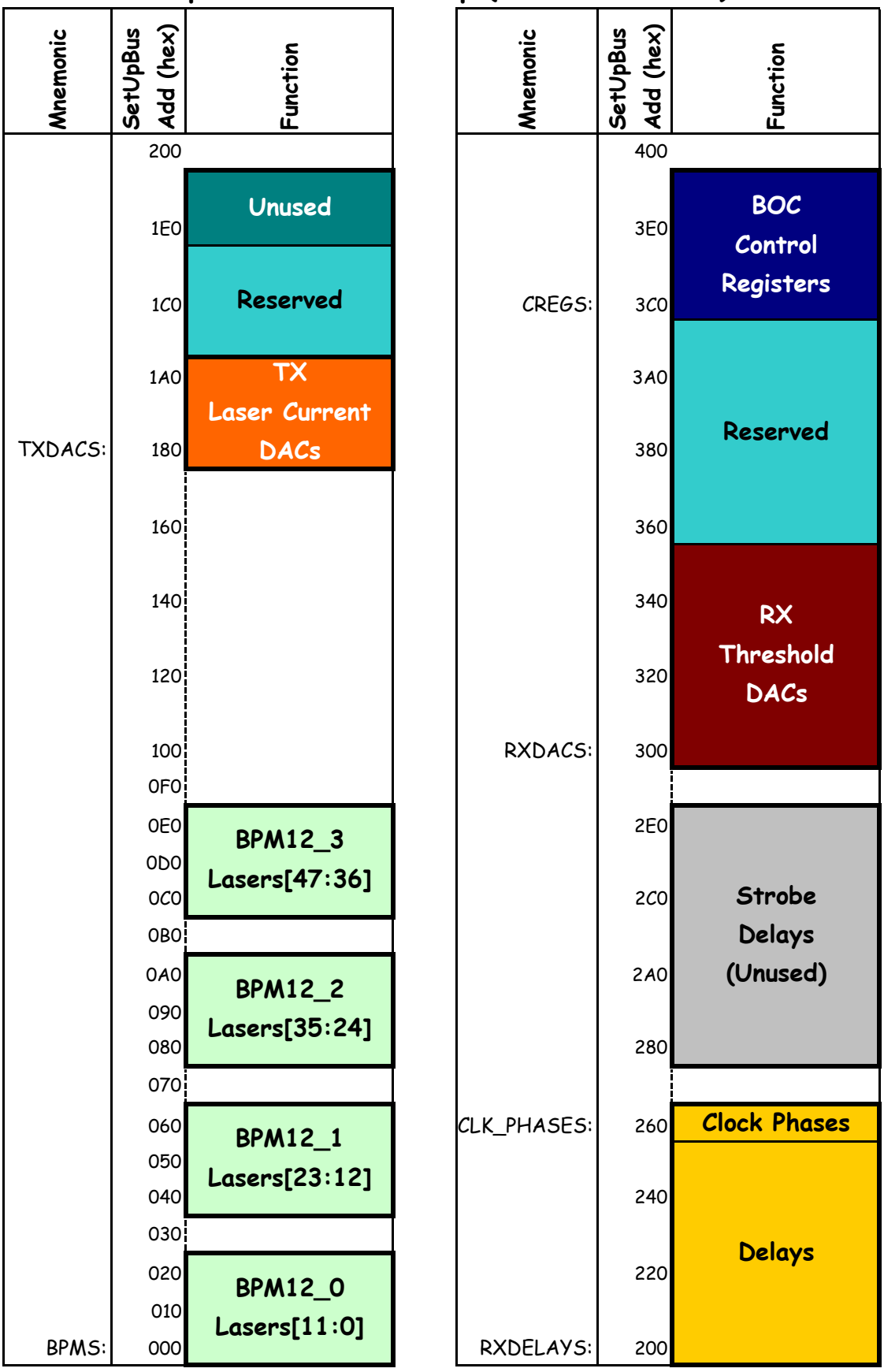
BOC1 Set-Up Bus

Top Level Address Map (Atlas User View)



BPM12 Registers (BPM12 Registers are Read-Write)

Address Offset (Hex)	Relative Laser #	Function	Bits	Reset Value (Hex)
+2F	11	Fine Delay	6:0	0
+2E	11	Coarse Delay	4:0	0
+2D	11	Mark-Space	4:0	13 (~50%)
+2C	11	Stream Inhibit	0:0	0 (=Enabled)
+2B	10	Fine Delay	6:0	0
+2A	10	Coarse Delay	4:0	0
+29	10	Mark-Space	4:0	13 (~50%)
+28	10	Stream Inhibit	0:0	0 (=Enabled)
+27	9	Fine Delay	6:0	0
+26	9	Coarse Delay	4:0	0
+25	9	Mark-Space	4:0	13 (~50%)
+24	9	Stream Inhibit	0:0	0 (=Enabled)
+23	8	Fine Delay	6:0	0
+22	8	Coarse Delay	4:0	0
+21	8	Mark-Space	4:0	13 (~50%)
+20	8	Stream Inhibit	0:0	0 (=Enabled)
+1F	7	Fine Delay	6:0	0
+1E	7	Coarse Delay	4:0	0
+1D	7	Mark-Space	4:0	13 (~50%)
+1C	7	Stream Inhibit	0:0	0 (=Enabled)
+1B	6	Fine Delay	6:0	0
+1A	6	Coarse Delay	4:0	0
+19	6	Mark-Space	4:0	13 (~50%)
+18	6	Stream Inhibit	0:0	0 (=Enabled)
+17	5	Fine Delay	6:0	0
+16	5	Coarse Delay	4:0	0
+15	5	Mark-Space	4:0	13 (~50%)
+14	5	Stream Inhibit	0:0	0 (=Enabled)
+13	4	Fine Delay	6:0	0
+12	4	Coarse Delay	4:0	0
+11	4	Mark-Space	4:0	13 (~50%)
+10	4	Stream Inhibit	0:0	0 (=Enabled)
+0F	3	Fine Delay	6:0	0
+0E	3	Coarse Delay	4:0	0
+0D	3	Mark-Space	4:0	13 (~50%)
+0C	3	Stream Inhibit	0:0	0 (=Enabled)
+0B	2	Fine Delay	6:0	0
+0A	2	Coarse Delay	4:0	0
+09	2	Mark-Space	4:0	13 (~50%)
+08	2	Stream Inhibit	0:0	0 (=Enabled)
+07	1	Fine Delay	6:0	0
+06	1	Coarse Delay	4:0	0
+05	1	Mark-Space	4:0	13 (~50%)
+04	1	Stream Inhibit	0:0	0 (=Enabled)
+03	0	Fine Delay	6:0	0
+02	0	Coarse Delay	4:0	0
+01	0	Mark-Space	4:0	13 (~50%)
+00	0	Stream Inhibit	0:0	0 (=Enabled)

Laser Current DACs (see note below)					
SetUp BUS ADDRESS	Laser Number	Technical Detail			
		TX MDAC #	MD_SEL	PAL	MD_SADD
1AF	47	TXMD7	0x17	TX_MDPAL	2
1AE	46				3
1AD	45				4
1AC	44				5
1AB	43				6
1AA	42				7
1A9	41	TXMD6	0x16		2
1A8	40				3
1A7	39				4
1A6	38				5
1A5	37				6
1A4	36				7
1A3	35	TXMD5	0x15		2
1A2	34				3
1A1	33				4
1A0	32				5
19F	31				6
19E	30				7
19D	29	TXMD4	0x14		2
19C	28				3
19B	27				4
19A	26				5
199	25				6
198	24				7
197	23	TXMD3	0x13		2
196	22				3
195	21				4
194	20				5
193	19				6
192	18				7
191	17	TXMD2	0x12		2
190	16				3
18F	15				4
18E	14				5
18D	13				6
18C	12				7
18B	11	TXMD1	0x11		2
18A	10				3
189	9				4
188	8				5
187	7				6
186	6				7
185	5	TXMD0	0x10		2
184	4				3
183	3				4
182	2				5
181	1				6
180	0				7

Note: TX Laser Current DACs have a threshold:
0mA up to around 150, then linear to around 18mA at 255

RX Delays and Clock Phases (0-24 in 1ns steps)					
SetUp BUS ADDRESS	Function	Technical Detail			
		Delay Chip #	A[5:2]	S[2:0]	I2C-Bus
2FF	None	None	X	X	None
^	^	^	^	^	^
2E9	None	None	X	X	None
2E8	None				
2E7	None	PHOS4_25	9	7	I2C-Bus1
2E6	None			6	
2E5	None			5	
2E4	StrobeDelay25			4	
2E3	None	PHOS4_24	8	7	
2E2	None			6	
2E1	None			5	
2E0	StrobeDelay24			4	
2DF	None	PHOS4_23	7	7	
2DE	None			6	
2DD	None			5	
2DC	StrobeDelay23			4	
^	^	^	^	^	
2C3	None	PHOS4_16	0	7	
2C2	None			6	
2C1	None			5	
2C0	StrobeDelay16			4	
2BF	None	PHOS4_15	F	7	I2C-Bus0
2BE	None			6	
^	^	^	^	^	
287	None	PHOS4_1	1	7	
286	None			6	
285	None			5	
284	StrobeDelay1			4	
283	None	PHOS4_0	0	7	
282	None			6	
281	None			5	
280	StrobeDelay0			4	
^	^	^	^	^	^
269	None	None	X	X	None
268					
267	Not Used	PHOS4_25	9	3	I2C-Bus1
266	Not Used			2	
265	VernierClock_StepPhase1			1	
264	VernierClock_StepPhase0			0	
263	B-Reg Clock Phase	PHOS4_24	8	3	
262	Not Used			2	
261	Not Used			1	
260	BPM Clock Phase			0	
25F	DataDelay95	PHOS4_23	7	3	
25E	DataDelay94			2	
^	^	^	^	^	
245	DataDelay69	PHOS4_17	1	1	
244	DataDelay68			0	
243	DataDelay67	PHOS4_16	0	3	
242	DataDelay66			2	
241	DataDelay65			1	
240	DataDelay64			0	
23F	DataDelay63	PHOS4_15	F	3	I2C-Bus0
23E	DataDelay62			2	
^	^	^	^	^	
209	DataDelay9	PHOS4_2	2	1	
208	DataDelay8			0	
207	DataDelay7	PHOS4_1	1	3	
206	DataDelay6			2	
205	DataDelay5			1	
204	DataDelay4			0	
203	DataDelay3	PHOS4_0	0	3	
202	DataDelay2			2	
201	DataDelay1			1	
200	DataDelay0			0	

Note 1 : BOC currently makes no use of Strobe Delays, so top used RXDelay SUB Address is 265 hex

Note 2 : The 2 VernierClock_StepPhases add to give a range of 0-50ns in 1ns steps

First Bank of RX Threshold DACs (0:255 for 0 to 255 uA)					
SetUp BUS ADDRESS	Data Stream Number	Technical Detail			
		RX MDAC #	MD_SEL	PAL	MD_SADD
32F	47	RXMD7	0x07	RX_MDPAL0	2
32E	46	RXMD6	0x06		2
32D	45	RXMD7	0x07		3
32C	44	RXMD6	0x06		3
32B	43	RXMD7	0x07		4
32A	42	RXMD6	0x06		4
329	41	RXMD7	0x07		5
328	40	RXMD6	0x06		5
327	39	RXMD7	0x07		6
326	38	RXMD6	0x06		6
325	37	RXMD7	0x07		7
324	36	RXMD6	0x06		7
323	35	RXMD5	0x05		2
322	34	RXMD4	0x04		2
321	33	RXMD5	0x05		3
320	32	RXMD4	0x04		3
31F	31	RXMD5	0x05		4
31E	30	RXMD4	0x04		4
31D	29	RXMD5	0x05		5
31C	28	RXMD4	0x04		5
31B	27	RXMD5	0x05		6
31A	26	RXMD4	0x04		6
319	25	RXMD5	0x05		7
318	24	RXMD4	0x04		7
317	23	RXMD3	0x03		2
316	22	RXMD2	0x02		2
315	21	RXMD3	0x03		3
314	20	RXMD2	0x02		3
313	19	RXMD3	0x03		4
312	18	RXMD2	0x02		4
311	17	RXMD3	0x03		5
310	16	RXMD2	0x02		5
30F	15	RXMD3	0x03		6
30E	14	RXMD2	0x02		6
30D	13	RXMD3	0x03		7
30C	12	RXMD2	0x02		7
30B	11	RXMD1	0x01		2
30A	10	RXMD0	0x00		2
309	9	RXMD1	0x01		3
308	8	RXMD0	0x00		3
307	7	RXMD1	0x01		4
306	6	RXMD0	0x00		4
305	5	RXMD1	0x01		5
304	4	RXMD0	0x00		5
303	3	RXMD1	0x01		6
302	2	RXMD0	0x00		6
301	1	RXMD1	0x01		7
300	0	RXMD0	0x00		7

Second Bank of RX Threshold DACs (0:255 for 0 to 255 uA)					
SetUp BUS ADDRESS	Data Stream Number	Technical Detail			
		RX MDAC #	MD_SEL	PAL	MD_SADD
35F	95	RXMD15	0x0F	RX_MDPAL1	2
35E	94	RXMD14	0x0E		2
35D	93	RXMD15	0x0F		3
35C	92	RXMD14	0x0E		3
35B	91	RXMD15	0x0F		4
35A	90	RXMD14	0x0E		4
359	89	RXMD15	0x0F		5
358	88	RXMD14	0x0E		5
357	87	RXMD15	0x0F		6
356	86	RXMD14	0x0E		6
355	85	RXMD15	0x0F		7
354	84	RXMD14	0x0E		7
353	83	RXMD13	0x0D		2
352	82	RXMD12	0x0C		2
351	81	RXMD13	0x0D		3
350	80	RXMD12	0x0C		3
34F	79	RXMD13	0x0D		4
34E	78	RXMD12	0x0C		4
34D	77	RXMD13	0x0D		5
34C	76	RXMD12	0x0C		5
34B	75	RXMD13	0x0D		6
34A	74	RXMD12	0x0C		6
349	73	RXMD13	0x0D		7
348	72	RXMD12	0x0C		7
347	71	RXMD11	0x0B		2
346	70	RXMD10	0x0A		2
345	69	RXMD11	0x0B		3
344	68	RXMD10	0x0A		3
343	67	RXMD11	0x0B		4
342	66	RXMD10	0x0A		4
341	65	RXMD11	0x0B		5
340	64	RXMD10	0x0A		5
33F	63	RXMD11	0x0B		6
33E	62	RXMD10	0x0A		6
33D	61	RXMD11	0x0B		7
33C	60	RXMD10	0x0A		7
33B	59	RXMD9	0x09		2
33A	58	RXMD8	0x08		2
339	57	RXMD9	0x09		3
338	56	RXMD8	0x08		3
337	55	RXMD9	0x09		4
336	54	RXMD8	0x08		4
335	53	RXMD9	0x09		5
334	52	RXMD8	0x08		5
333	51	RXMD9	0x09		6
332	50	RXMD8	0x08		6
331	49	RXMD9	0x09		7
330	48	RXMD8	0x08		7

BOC Controls						Comments
Addr	Read Function	Bits	Write Function	Label	Note	
3FF						
3FE						
3FD						
3FC						
3FB						
3FA						
3F9						
3F8						
3F7						
3F6						
3F5						
3F4						
3F3						
3F2						
3F1						
3F0	Serial No. (board switches)	[7:0]	No Action	MOD_SN		
3EF						
3EE						
3ED						
3EC						
3EB						
3EA						
3E9						
3E8						
3E7						
3E6						
3E5						
3E4						
3E3	Manufacturer = CB (hex)	[7:0]	No Action	MANUF		was MS of 2
3E2	Module Type = 44 (dec)	[7:0]	No Action	MOD_TYPE		moved, was 39
3E1	Hardware Revision	[7:0]	No Action	HW_REV		new
3E0	Firmware Revision	[7:0]	No Action	FIRM_REV		moved, renamed
3DF						
3DE						
3CD						
3DC						
3DB						
3DA						
3D9						
3D8						
3D7						
3D6						
3D5						
3D4						
3D3						
3D2	Clock Control Bits	[3:0]	Clock Control Bits	CK_CONT	[1]	changed
3D1	Reserved		Reserved			changed
3D0	Vernier Clock Fine Phase	[7:0]	Vernier Clock Fine Phase	VC_FPh	[2]	changed,renamed
3CF						removed
3CE						removed
3CD						
3CC						
3CB	RX Data Mode	[2:0]	RX Data Mode	RXDMODE		was 2 bits
3CA						removed
3C9	RX DAC Clear	[0:0]	RX DAC Clear	RXDCLR		
3C8	TX DAC Clear	[0:0]	TX DAC Clear	TXDCLR		
3C7						
3C6						
3C5						
3C4	BPM Reset	[0:0]	BPM Reset	BPMRST		
3C3						
3C2						
3C1	BOC Status	[0:0]	No Action	BOCSTAT		
3C0	BOC Reset	[0:0]	BOC Reset	BOCRST		

Notes [1] Clock Control word: [BPMPh_Bypass,VernierStep_Bypass,Half_Clock,Clock_Invert]

[2] Vernier Clock Fine Phase [7:0] sets delay in 40ps steps (0-2Ons)

Revision Record		
Date	**Sheets Affected**	**Note**
15-Feb-00	Notes	Sheet created
15-Feb-00	BOC Controls	Sheet created: all "To Be Assigned"
15-Feb-00	RX_Delays	Map completed
15-Feb-00	TOP	Transferred from Word document: Delays extended to 2FF
20-Nov-00	All	Create BOC-RIG_add_maps.xls from BOC add_maps
22-Jan-01	All	re-created BOC0_add_maps from BOB-RIG_add_maps
31-Jan-01	TXDACs,BOC Controls	Updated
01-Mar-01	All	Added BPMs - ordered sheets by address
01-Mar-01	TOP	Made specific to BOC0; Address Mnemonics added
11-Jul-01	ALL	Created BOC1 Add Map from BOC0
19-Apr-02	ALL	Updated info, added VME Addresses (Hide for User Version)
23-Apr-02	ALL	Custom Views "All" and "Atlas User" created. Typos fixed on "BPM"

Notes	
Sheets Affected	**Note**