SHEET1 = THIS SHEET
SHEET2 = JI/JTAG/I2C/MISC
SHEET3 = USB - ETH + XTAL OSC
SHEET4 = TTCRX
SHEET5 = 3 X 12 CHANNEL RX
SHEET6 = FPGA1 ROCKETS + PROM1
SHEET7 = FPGA2 ROCKETS + PROM2
SHEET8 = FPGA3 ROCKETS + PROM3
SHEET9 = FPGA4 ROCKETS + PROM4
SHEET10 = FPGA5 ROCKETS + PROM5
SHEET11 = FPGA1 BANKS 0/1/4 + 5 = RAM CONTROL
SHEET12 = FPGA1 BANKS 2/3 = TTCRX/USB/ETH
SHEET13 = FPGA1 BANKS 6/7 = RAM 1-4 CONTROL
SHEET14 = FPGA2 BANKS 0/1/4 + 5 = RAMCONTROL
SHEET15 = FPGA2 BANKS 2/3 = RAM 7-9 CONTROL
SHEET16 = FPGA2 BANKS 6/7 = RAM 1-6 CONTROL
SHEET17 = FPGA3 BANKS 0/1/4 + 5 = RAM CONTROL
SHEET18 = FPGA3 BANKS 2/3 = RAM 7-9 CONTROL
SHEET19 = FPGA3 BANKS 6/7 = RAM 1-6 CONTROL
SHEET20 = FPGA4 BANKS 0/1/4 + 5 = RAM CONTROL
SHEET21 = FPGA4 BANKS 2/3 = RAM 7-9 CONTROL
SHEET22 = FPGA4 BANKS 6/7 = RAM 1-6 CONTROL
SHEET23 = FPGA5 BANKS 0/1/4 + 5 = RAM CONTROL
SHEET24 = FPGA5 BANKS 2/3 = RAM 7-9 CONTROL
SHEET25 = FPGA5 BANKS 6/7 = RAM 1-6 CONTROL
SHEET26 = RAMS 1-4 (FPGA1)
SHEET27 = RAMS 1-9 (FPGA2)
SHEET28 = RAMS 1-9 (FPGA3)
SHEET29 = RAMS 1-9 (FPGA4)
SHEET30 = RAMS 1-9 (FPGA5)
SHEET31 = 4 X TXRX (AGILENT)
SHEET32 = QUAD GBE
SHEET33 = GLUE CARD
SHEET34 = CREDIT CARD PC
SHEET35 = CLOCKS - SYSTEM=80.440MHZ - REFERENCE=80.157MHZ
SHEET36 = VOLTAGE REGULATORS - AREA 1
SHEET37 = VOLTAGE REGULATORS - AREA 2
SHEET38 = VOLTAGE REGULATORS - AREA 3
SHEET39 = VOLTAGE REGULATORS - AREA 4
SHEET40 = VOLTAGE REGULATORS - AREA 5
SHEET41 = 51R DISCRETE FPGA - RAM TERMINATIONS

PROPAGATION DELAY

TOP/BOTTOM	=	54.46	PS/CM
INTERNAL	=	68.37	PS/CM

BOARD BUILD

T
P1
G1
S1
S2
G2
P2
S3
S4
P3
G3
S5
S6
G4
P4
B

TRACK - GAP

50R	TOP/BOTTOM	=	6.00	MIL	= 0.1524MM
50R	INTERNAL	=	5.50	MIL	= 0.1397MM
100R	TRACK TOP/BOTTOM	=	4.50	MIL	= 0.1143MM
100R	GAP TOP/BOTTOM	=	8.30	MIL	= 0.2102MM
100R	TRACK INTERNAL	=	4.25	MIL	= 0.1080MM
100R	GAP INTERNAL	=	7.00	MIL	= 0.1778MM

DEVELOPMENT

DRAWING

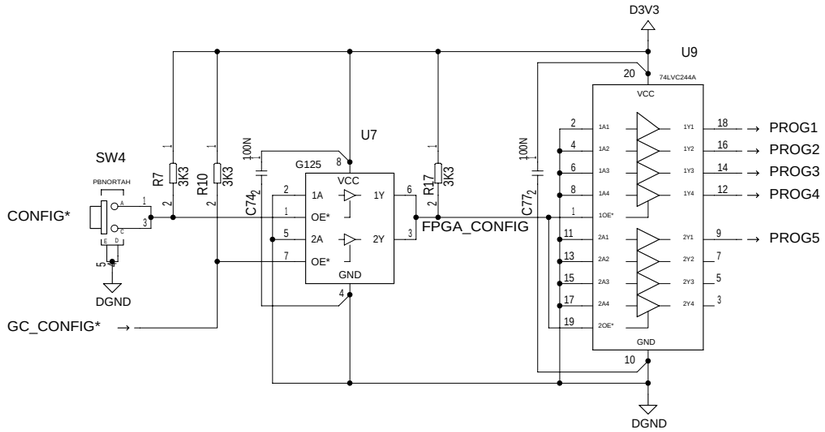
UNIVERSITY OF CAMBRIDGE HEP

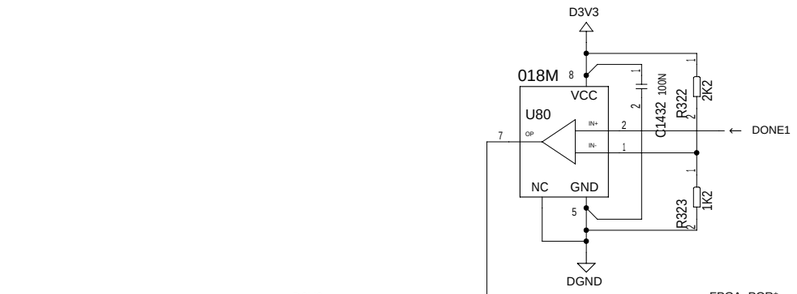
LHCB - RICHUKL1

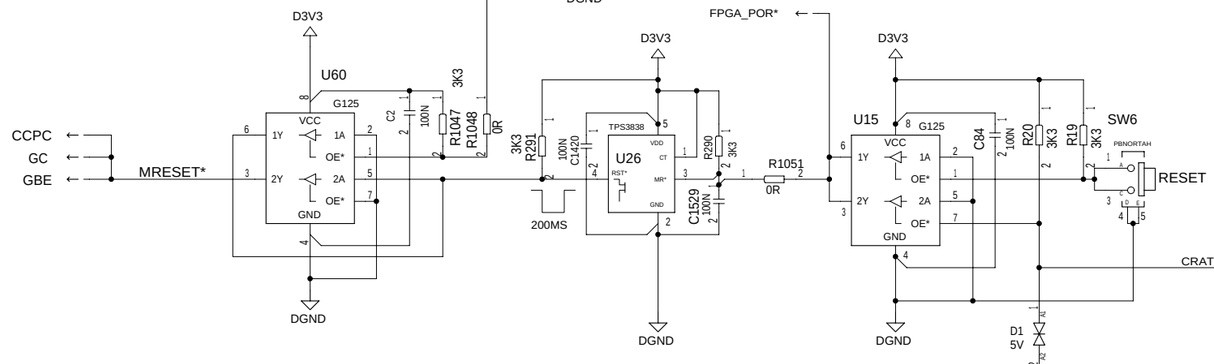
SCHEMATIC LISTING

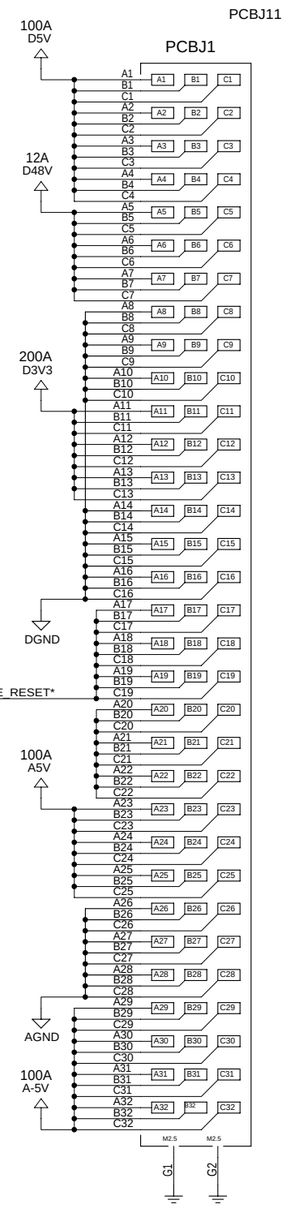
Thu Jun 08 08:37:22 2006

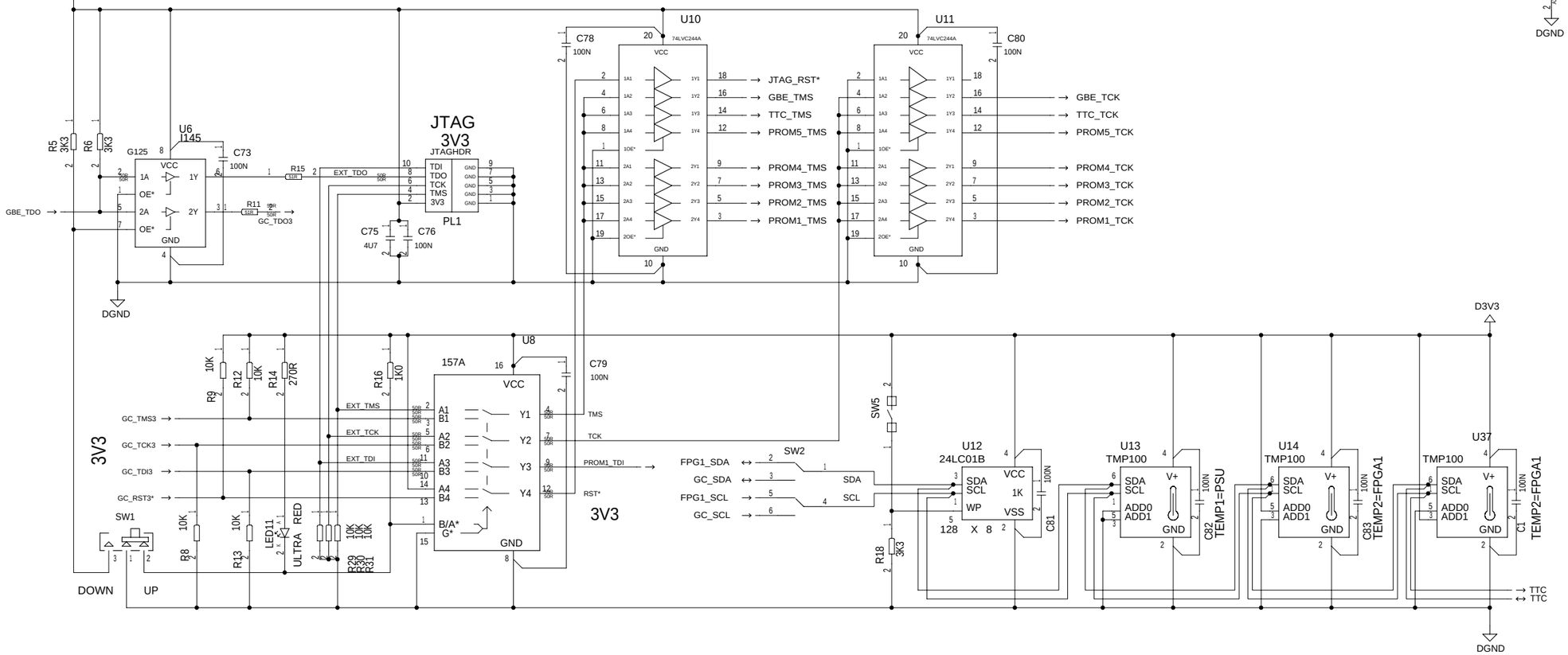
SHEET 1 OF 41







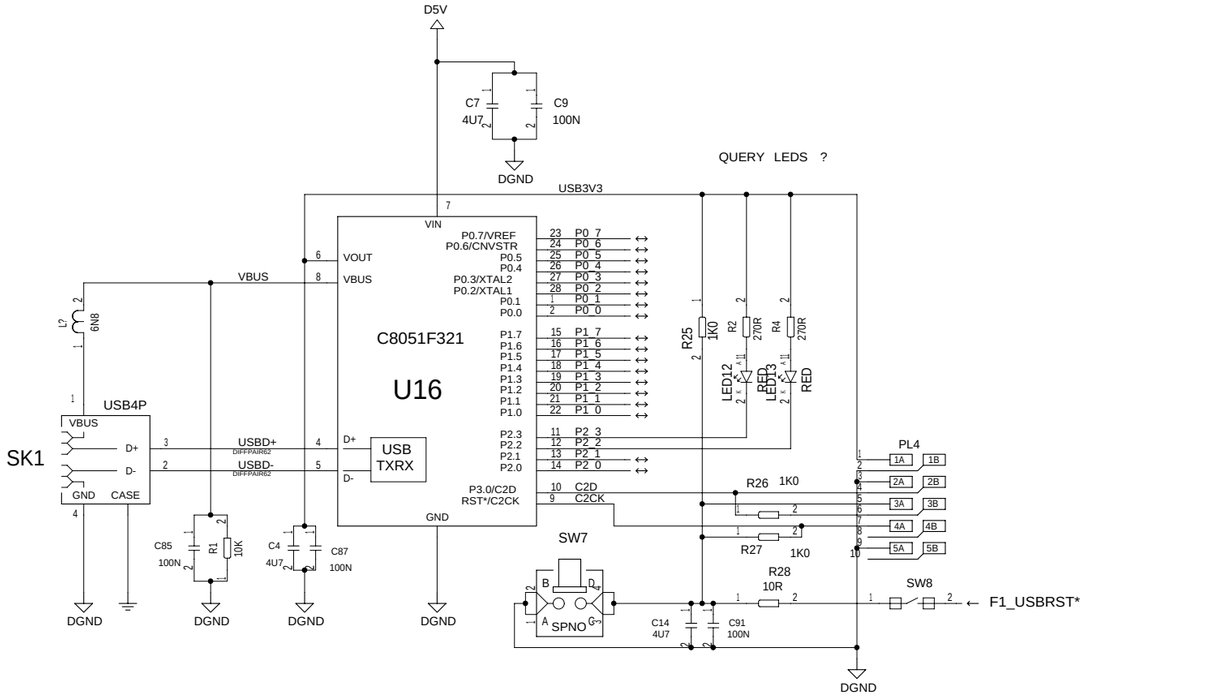




DEVELOPMENT

DRAWING

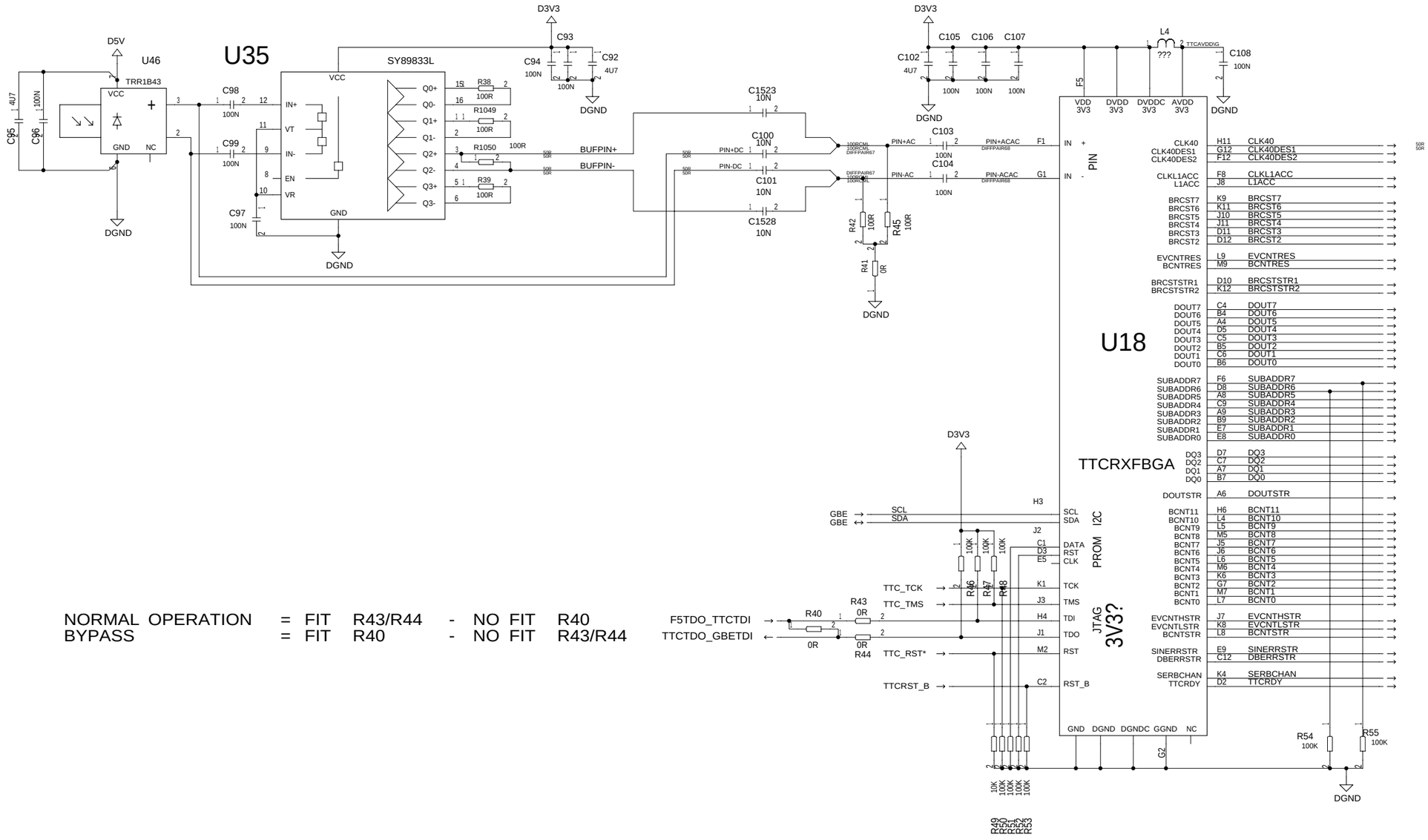
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
J1/JTAG/I2C/RESET/CONFIG		
Thu Jun 08 08:39:23 2006		
		SHEET 2 OF 41



DEVELOPMENT

DRAWING

UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
USB - ETH		
Thu Jun 08 08:41:47 2006		
		SHEET 3 OF 41

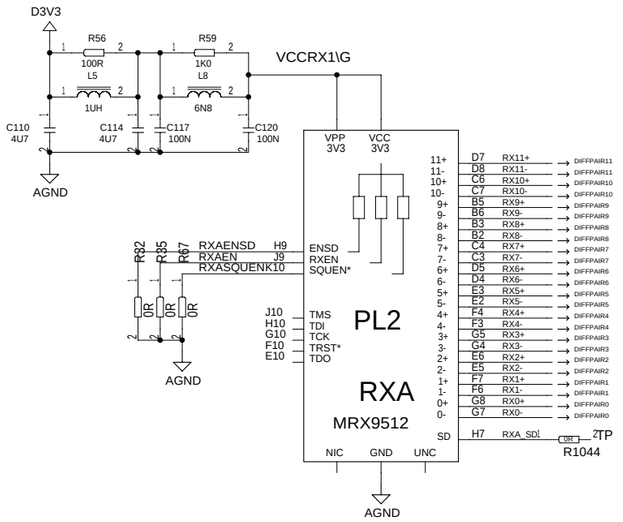


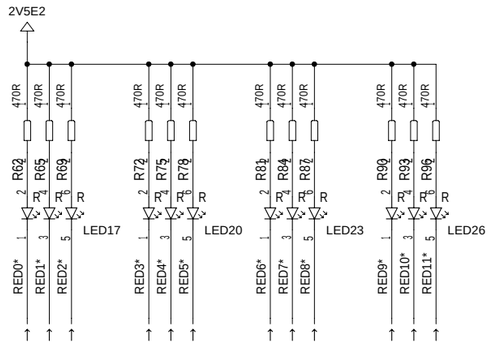
NORMAL OPERATION	=	FIT	R43/R44	-	NO FIT	R40	
BYPASS	=	FIT	R40	-	NO FIT	R43/R44	

DEVELOPMENT

DRAWING

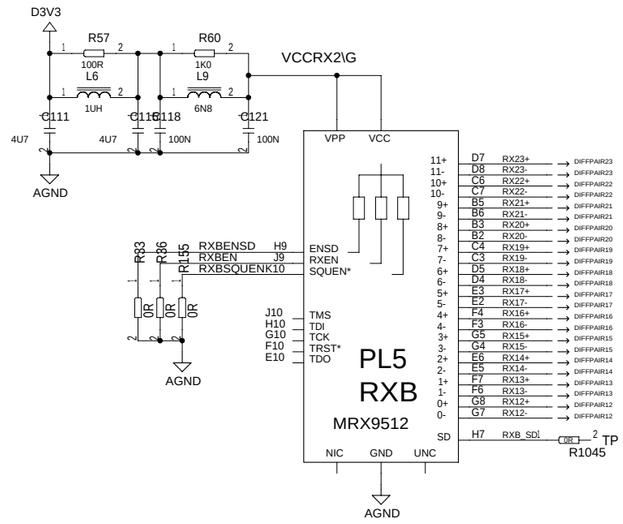
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
TTCRX		
Wed Jun 07 15:19:42 2006		
		SHEET 4 OF ??

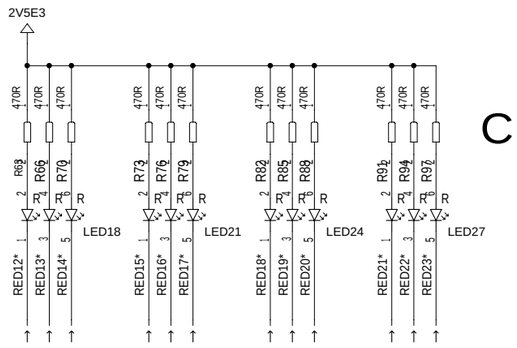




FPGA2

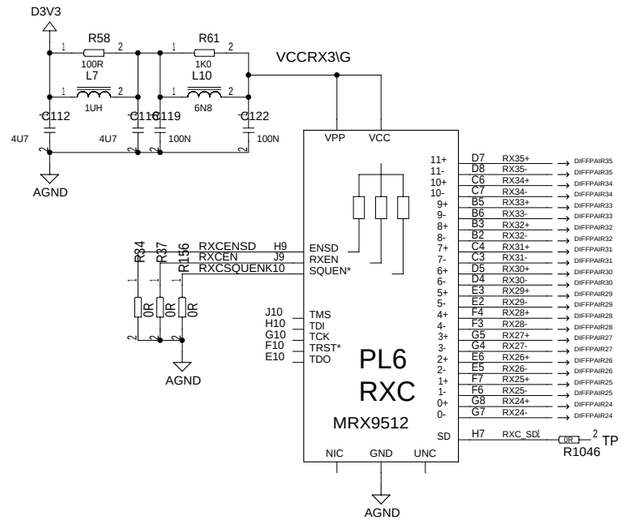
CHANGE 470R TO 100R

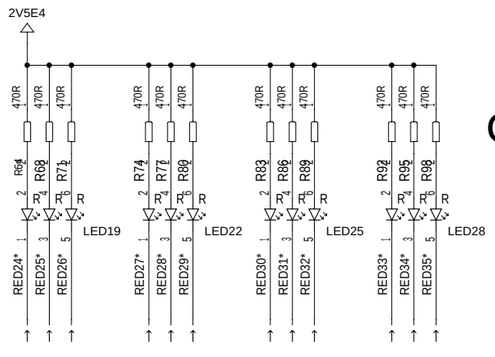




FPGA3

CHANGE 470R TO 100R





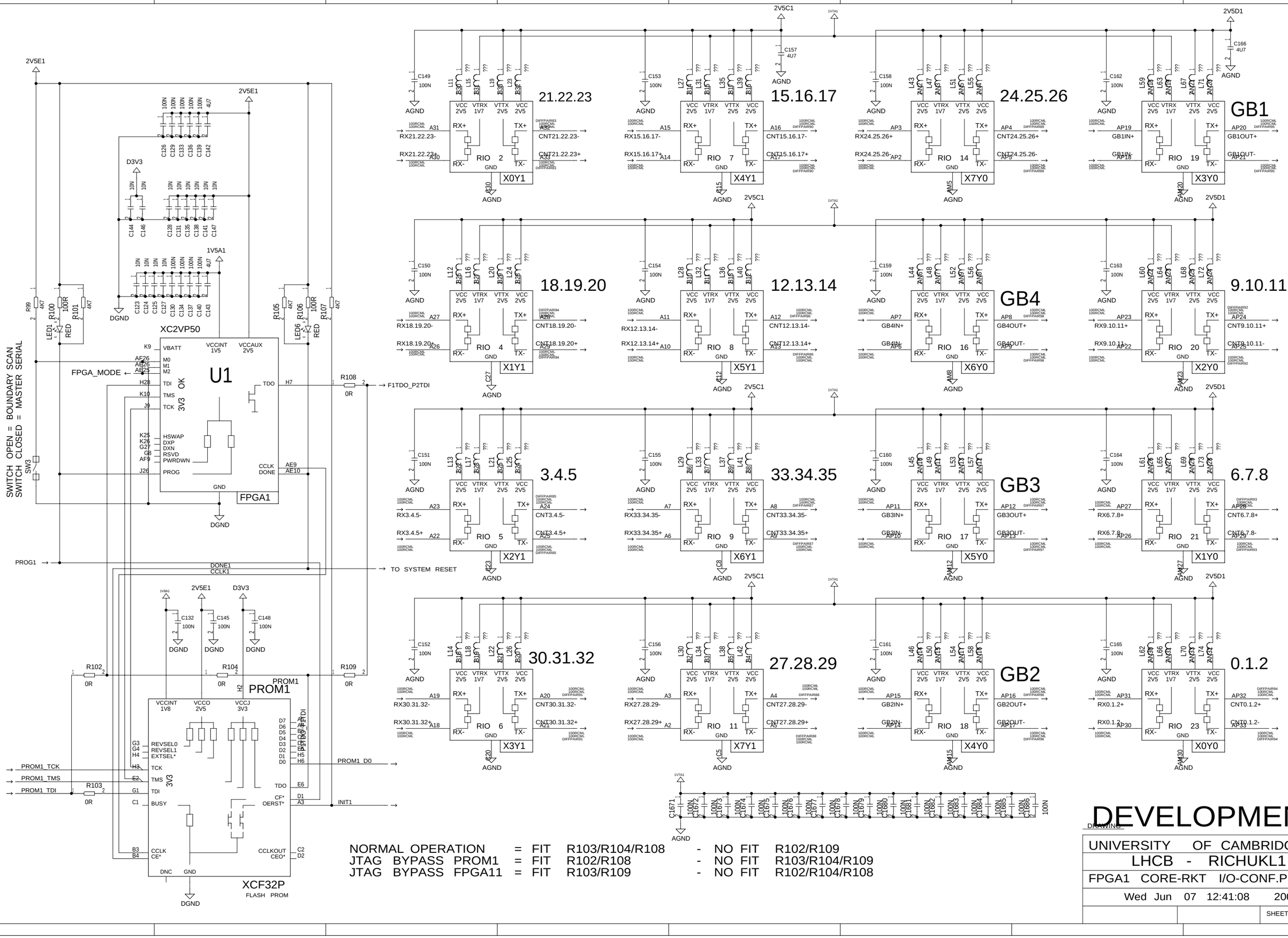
FPGA4

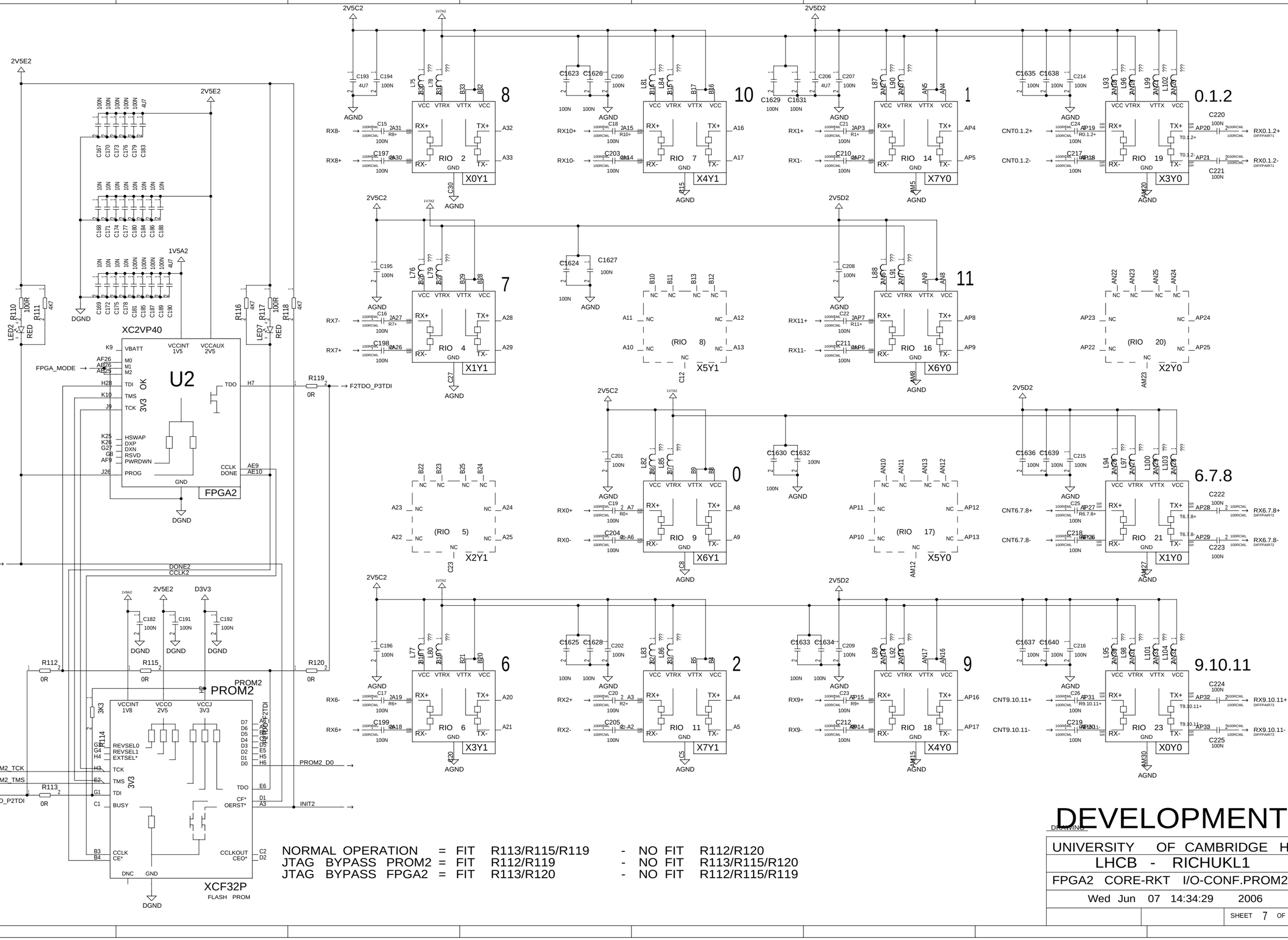
CHANGE 470R TO 100R

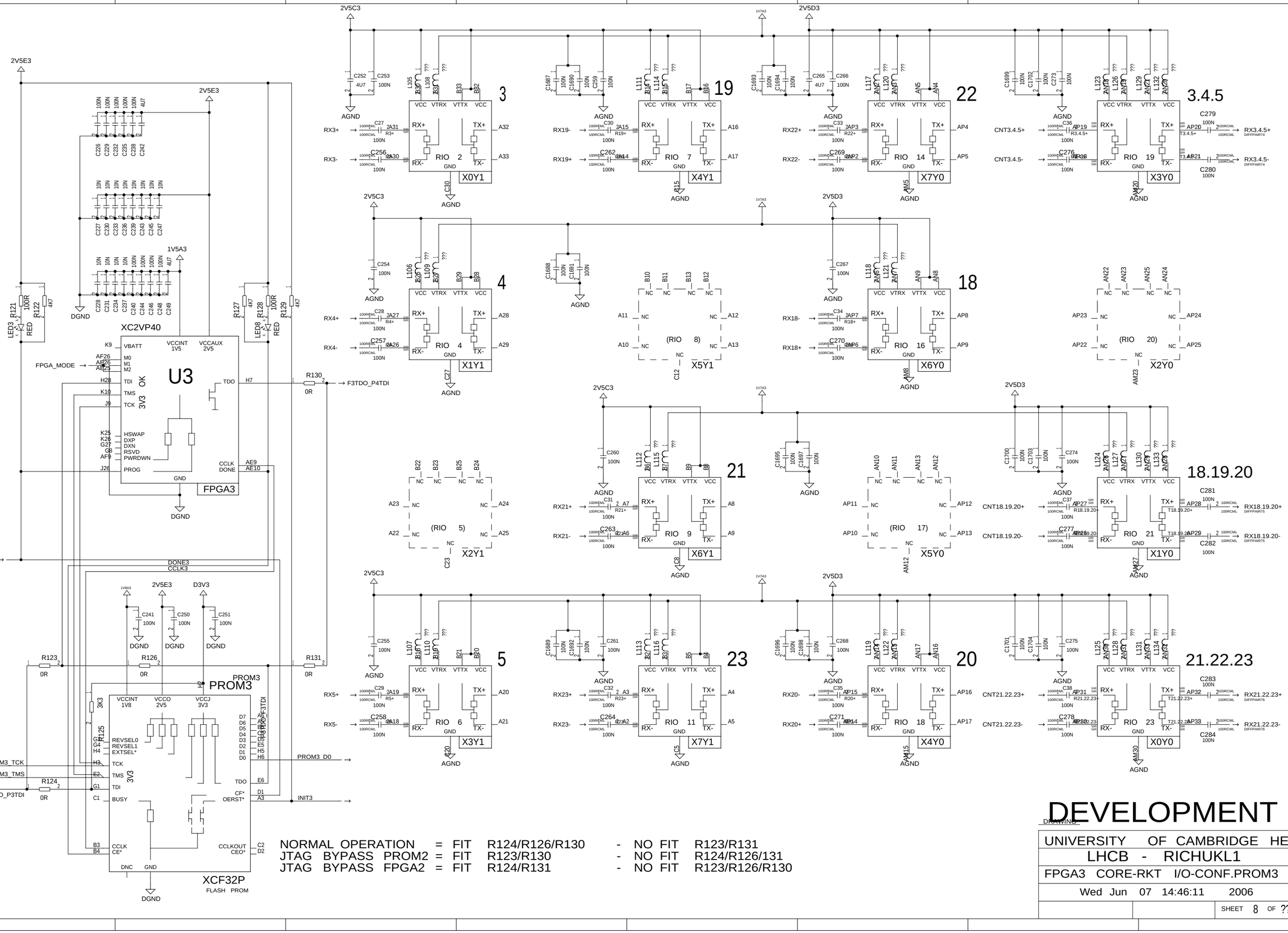
DEVELOPMENT

DRAWING

UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
3 X 12 CHANNEL RX		
Thu May 04 10:33:15 2006		
		SHEET 5 OF ??


SWITCH OPEN = BOUNDARY SCAN
SWITCH CLOSED = MASTER SERIAL
SW3
2V5E1
D3V3
1V5A1
DGND
XC2VP50
U1
FPGA1
VBATT
M0
M1
M2
TDI
TMS
TCK
HSWAP
DXP
DXN
RSVD
PWRDWN
PROG
TDO
CCLK
DONE
GND
OK
3V3
FPGA_MODE
→ F1TDO_P2TDI
PROG1
DONE1
CCLK1
→ TO SYSTEM RESET
PROM1
XCF32P
FLASH PROM
VCCINT 1V8
VCCO 2V5
VCCJ 3V3
REVSEL0
REVSEL1
EXTSEL*
BUSY
CCLK
CE*
CCLKOUT
CEO*
CF*
OERST*
DNC
PROM1_TCK
PROM1_TMS
PROM1_TDI
PROM1_D0
INIT1
2V5C1
2V5D1
1V7A1
21.22.23
15.16.17
24.25.26
GB1
18.19.20
12.13.14
GB4
9.10.11
3.4.5
33.34.35
GB3
6.7.8
30.31.32
27.28.29
GB2
0.1.2
RIO 2
RIO 7
RIO 14
RIO 19
RIO 4
RIO 8
RIO 16
RIO 20
RIO 5
RIO 9
RIO 17
RIO 21
RIO 6
RIO 11
RIO 18
RIO 23
X0Y1
X4Y1
X7Y0
X3Y0
X1Y1
X5Y1
X6Y0
X2Y0
X2Y1
X6Y1
X5Y0
X1Y0
X3Y1
X7Y1
X4Y0
X0Y0
RX21.22.23-
RX21.22.23+
CNT21.22.23-
CNT21.22.23+
RX15.16.17-
RX15.16.17+
CNT15.16.17-
CNT15.16.17+
RX24.25.26+
RX24.25.26-
CNT24.25.26+
CNT24.25.26-
GB1IN+
GB1IN-
GB1OUT+
GB1OUT-
RX18.19.20-
RX18.19.20+
CNT18.19.20-
CNT18.19.20+
RX12.13.14-
RX12.13.14+
CNT12.13.14-
CNT12.13.14+
GB4IN+
GB4IN-
GB4OUT+
GB4OUT-
RX9.10.11+
RX9.10.11-
CNT9.10.11+
CNT9.10.11-
RX3.4.5-
RX3.4.5+
CNT3.4.5-
CNT3.4.5+
RX33.34.35-
RX33.34.35+
CNT33.34.35-
CNT33.34.35+
GB3IN+
GB3IN-
GB3OUT+
GB3OUT-
RX6.7.8+
RX6.7.8-
CNT6.7.8+
CNT6.7.8-
RX30.31.32-
RX30.31.32+
CNT30.31.32-
CNT30.31.32+
RX27.28.29-
RX27.28.29+
CNT27.28.29-
CNT27.28.29+
GB2IN+
GB2IN-
GB2OUT+
GB2OUT-
RX0.1.2+
RX0.1.2-
CNT0.1.2+
CNT0.1.2-
R99
R100
R101
R102
R103
R104
R105
R106
R107
R108
R109
LED1
LED6
RED
0R
100R
4K7
NORMAL OPERATION = FIT R103/R104/R108 - NO FIT R102/R109
JTAG BYPASS PROM1 = FIT R102/R108 - NO FIT R103/R104/R109
JTAG BYPASS FPGA11 = FIT R103/R109 - NO FIT R102/R104/R108
DEVELOPMENT
DRAWING
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA1 CORE-RKT I/O-CONF.PROM1
Wed Jun 07 12:41:08 2006
SHEET 6 OF ??

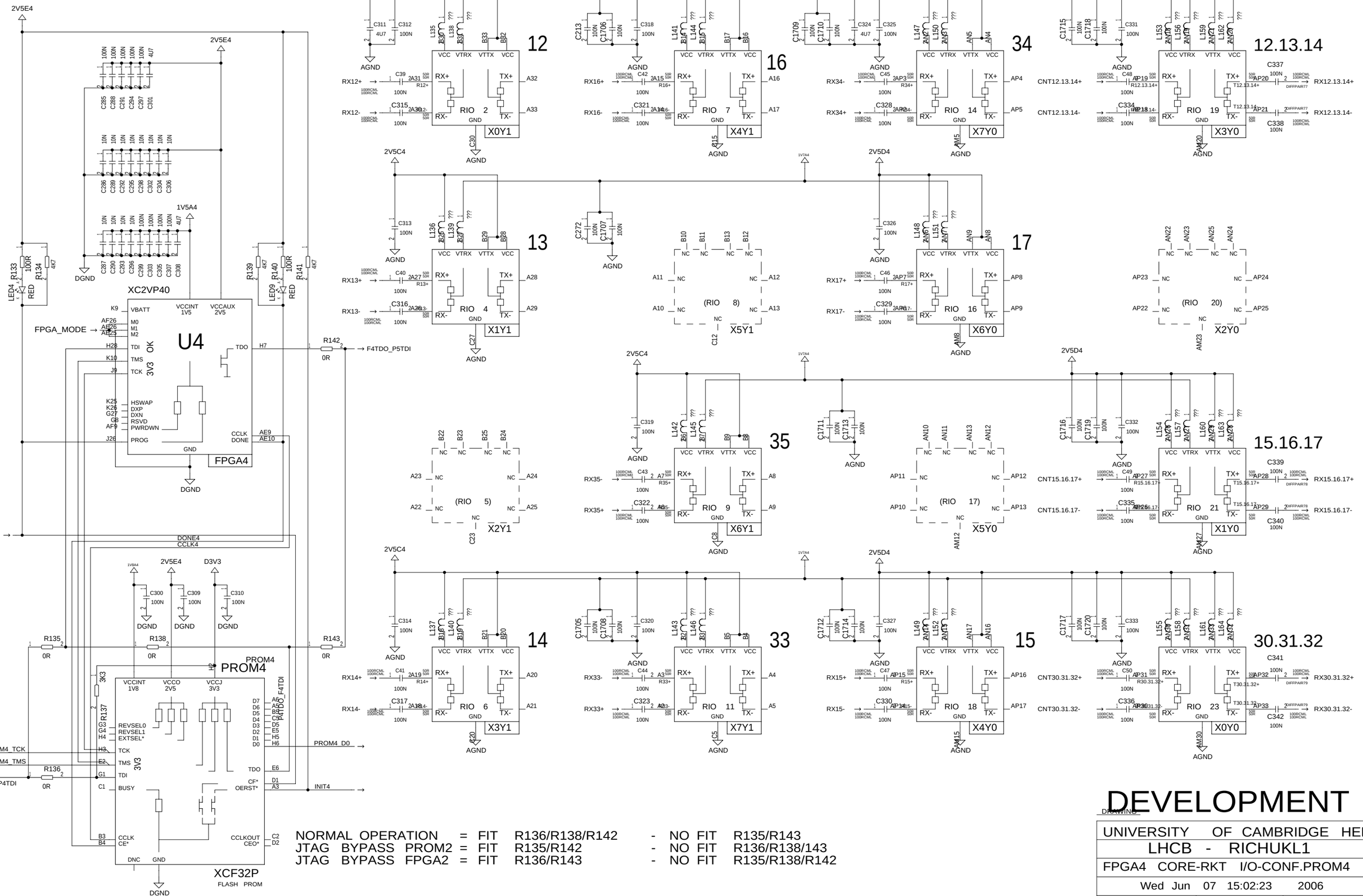

XC2VP40
U2
FPGA2
XCF32P
FLASH PROM
PROM2
RIO 2
RIO 7
RIO 14
RIO 19
RIO 4
RIO 16
(RIO 8)
RIO 6
RIO 11
RIO 18
RIO 23
(RIO 5)
RIO 9
RIO 21
(RIO 17)
(RIO 20)
X0Y1
X4Y1
X7Y0
X3Y0
X1Y1
X5Y1
X6Y0
X2Y1
X3Y1
X7Y1
X4Y1
X0Y0
X1Y0
X5Y0
X2Y0
8
10
1
0.1.2
7
11
6
2
9
9.10.11
0
6.7.8
F2TDO_P3TDI
F1TDO_P2TDI
PROG2
DONE2
CCLK2
PROM2_TCK
PROM2_TMS
PROM2_D0
INIT2
FPGA_MODE
NORMAL OPERATION = FIT R113/R115/R119 - NO FIT R112/R120
JTAG BYPASS PROM2 = FIT R112/R119 - NO FIT R113/R115/R120
JTAG BYPASS FPGA2 = FIT R113/R120 - NO FIT R112/R115/R119
DEVELOPMENT
DRAWING
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA2 CORE-RKT I/O-CONF.PROM2
Wed Jun 07 14:34:29 2006
SHEET 7 OF ??

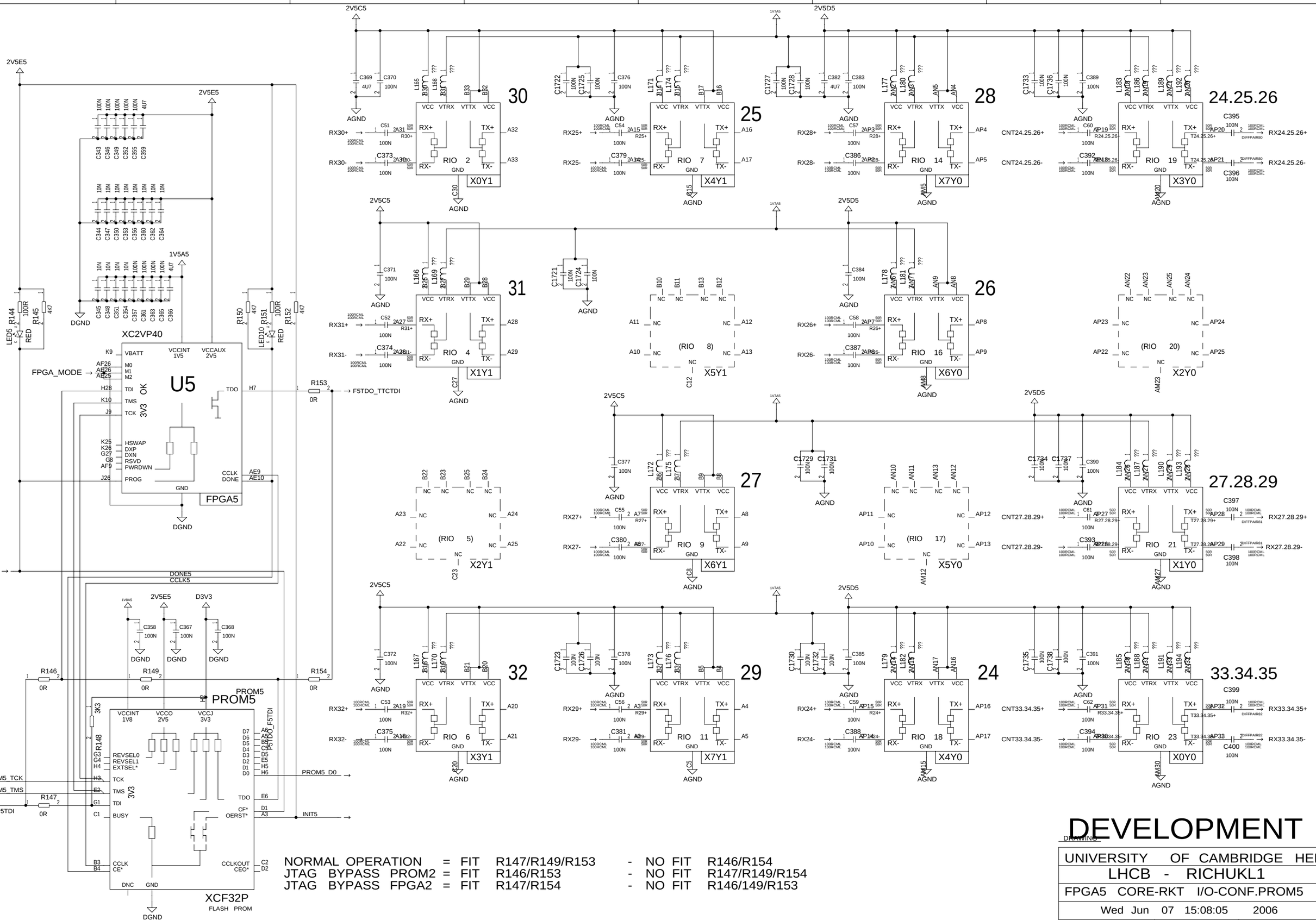


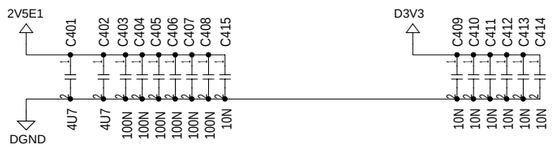
DEVELOPMENT

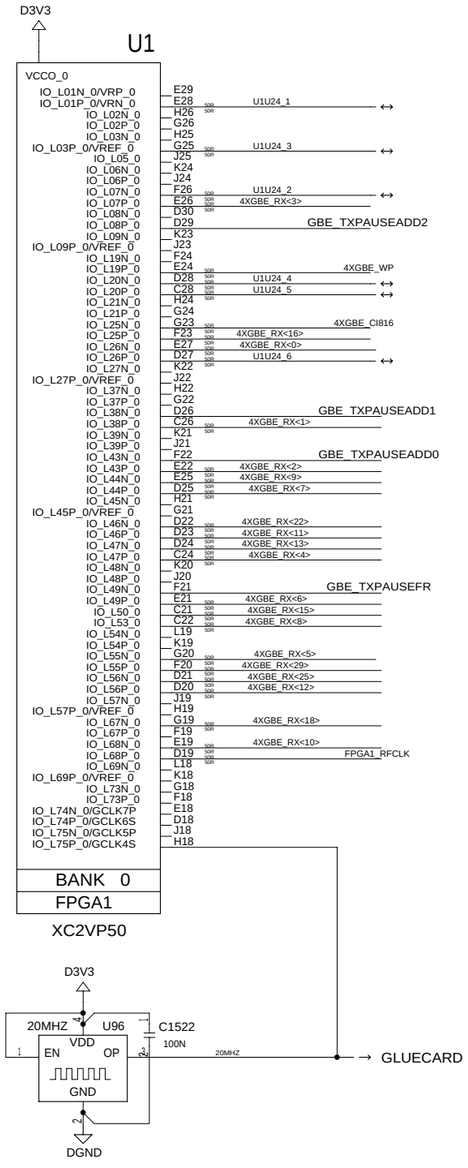
DRAWING

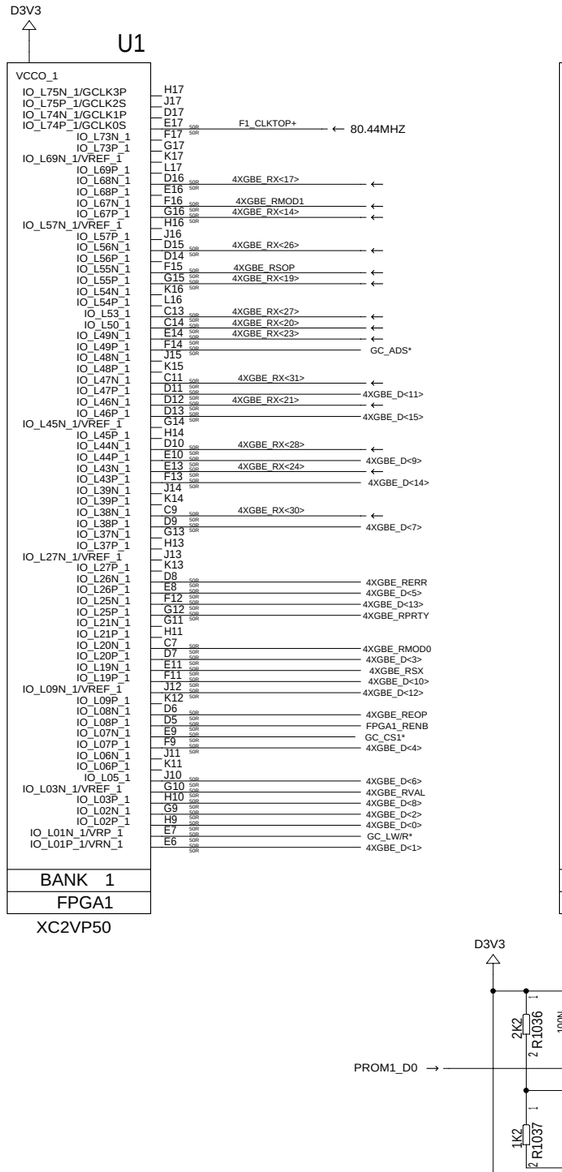
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA3 CORE-RKT I/O-CONF.PROM3		
Wed Jun 07 14:46:11 2006		
		SHEET 8 OF ??

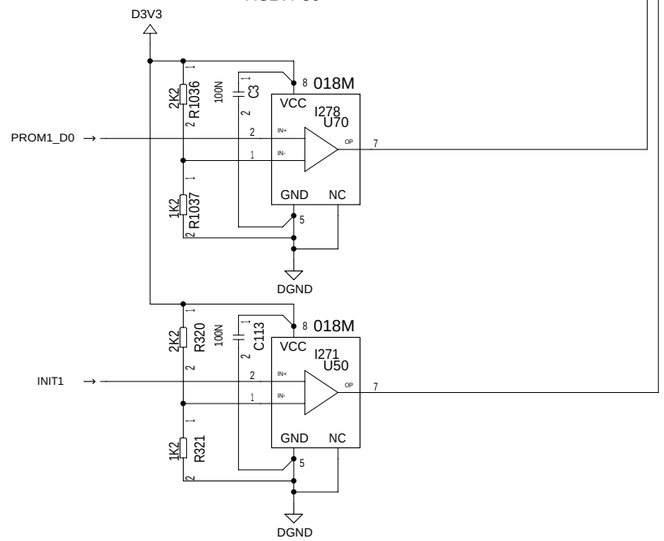

XC2VP40
U4
FPGA4
XCF32P
FLASH PROM
PROM4
FPGA_MODE
PROG4
DONE4
CCLK4
F4TDO_P5TDI
F3TDO_P4TDI
PROM4_TCK
PROM4_TMS
PROM4_D0
INIT4
12
13
14
15
16
17
33
34
35
12.13.14
15.16.17
30.31.32
X0Y1
X1Y1
X2Y1
X3Y0
X4Y1
X5Y1
X6Y0
X7Y0
X0Y0
X1Y0
X2Y0
X3Y1
X4Y0
X5Y0
X6Y1
X7Y1
NORMAL OPERATION = FIT R136/R138/R142 - NO FIT R135/R143
JTAG BYPASS PROM2 = FIT R135/R142 - NO FIT R136/R138/143
JTAG BYPASS FPGA2 = FIT R136/R143 - NO FIT R135/R138/R142
DEVELOPMENT
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA4 CORE-RKT I/O-CONF.PROM4
Wed Jun 07 15:02:23 2006
SHEET 9 OF ??

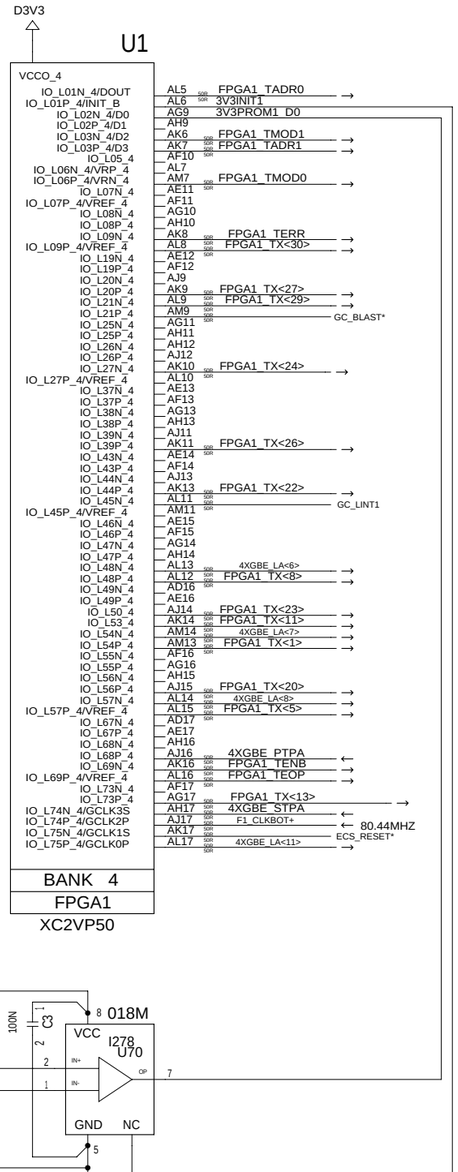

XC2VP40
U5
FPGA5
FPGA_MODE →
F5TDO_TTCTDI
PROG5 →
DONE5
CCLK5
PROM5
PROM5_TCK
PROM5_TMS
F4TDO_P5TDI
PROM5_D0
INIT5
XCF32P
FLASH PROM
NORMAL OPERATION = FIT R147/R149/R153 - NO FIT R146/R154
JTAG BYPASS PROM2 = FIT R146/R153 - NO FIT R147/R149/R154
JTAG BYPASS FPGA2 = FIT R147/R154 - NO FIT R146/149/R153
30
25
28
24.25.26
31
26
27
27.28.29
32
29
24
33.34.35
X0Y1
X4Y1
X7Y0
X3Y0
X1Y1
X5Y1
X6Y0
X2Y0
X2Y1
X6Y1
X5Y0
X1Y0
X3Y1
X7Y1
X4Y0
X0Y0
DEVELOPMENT
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA5 CORE-RKT I/O-CONF.PROM5
Wed Jun 07 15:08:05 2006
SHEET 10 OF ??

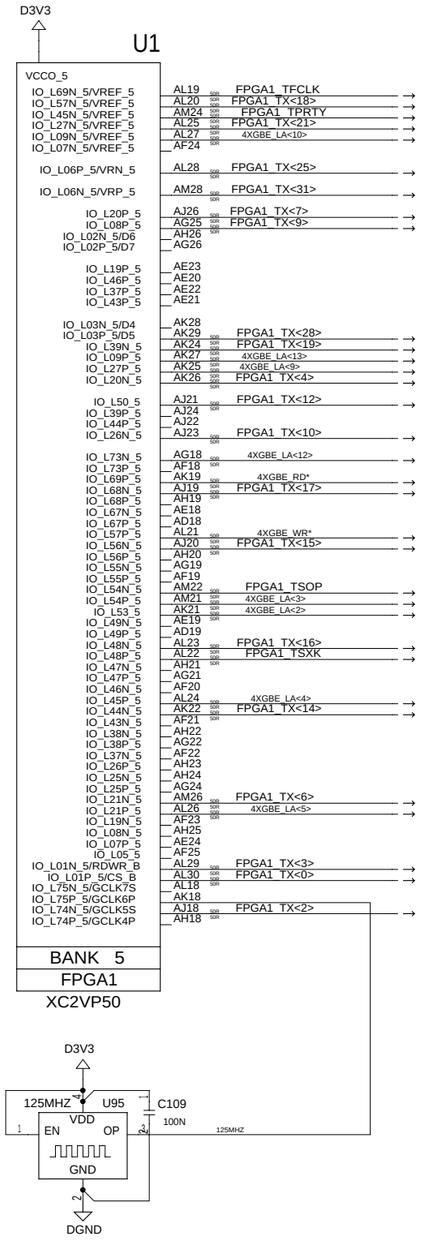








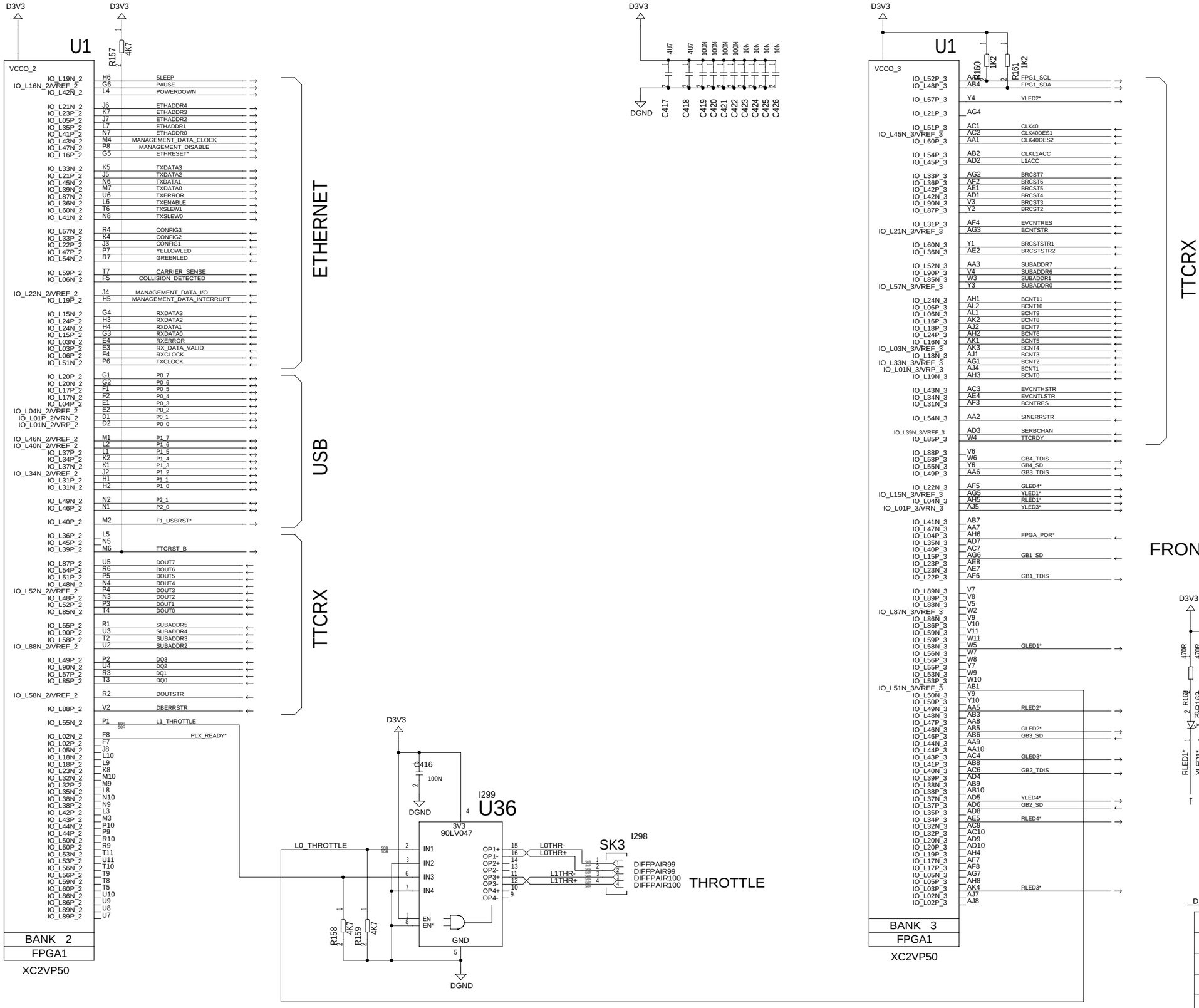




DEVELOPMENT

DRAWING

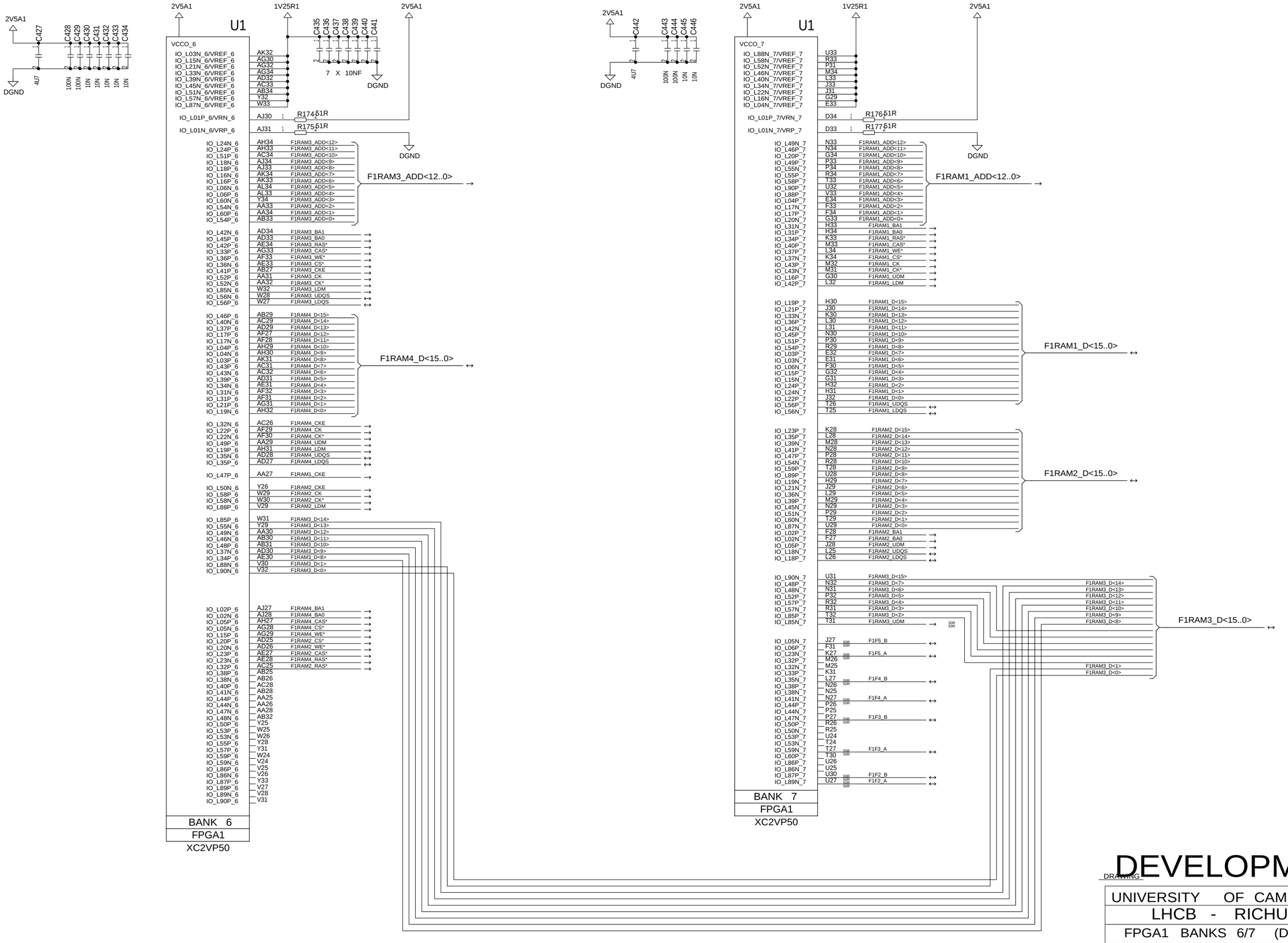
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA1 BANKS 0/1/4/5		
Wed May 03 09:14:07 2006		
		SHEET 11 OF ??

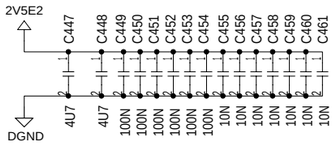


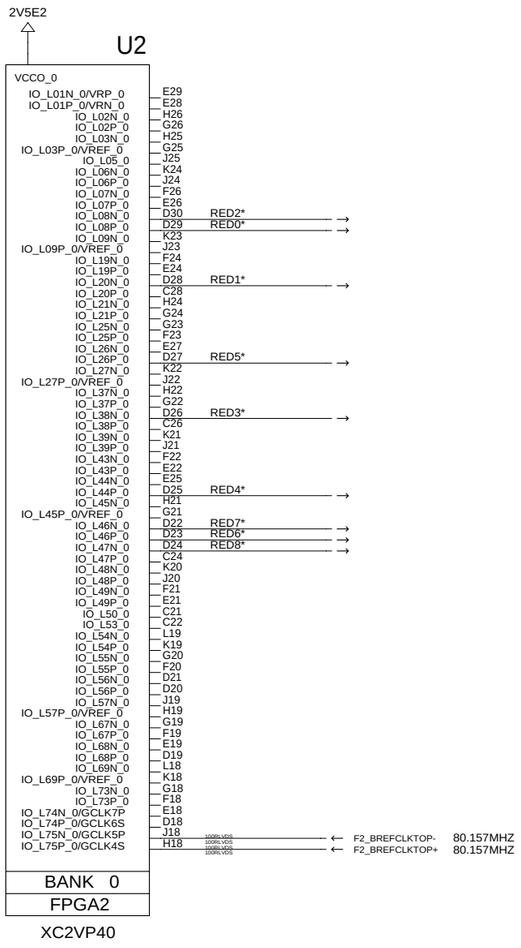
DEVELOPMENT

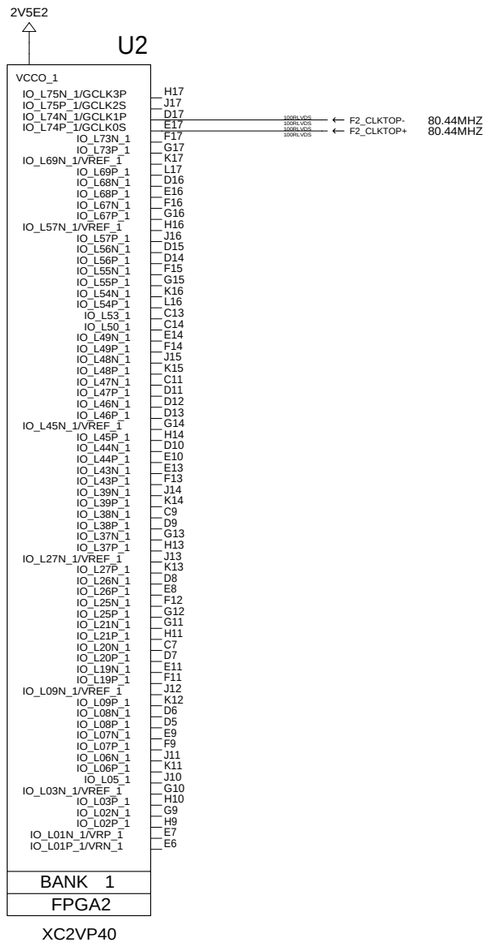
DRAWING

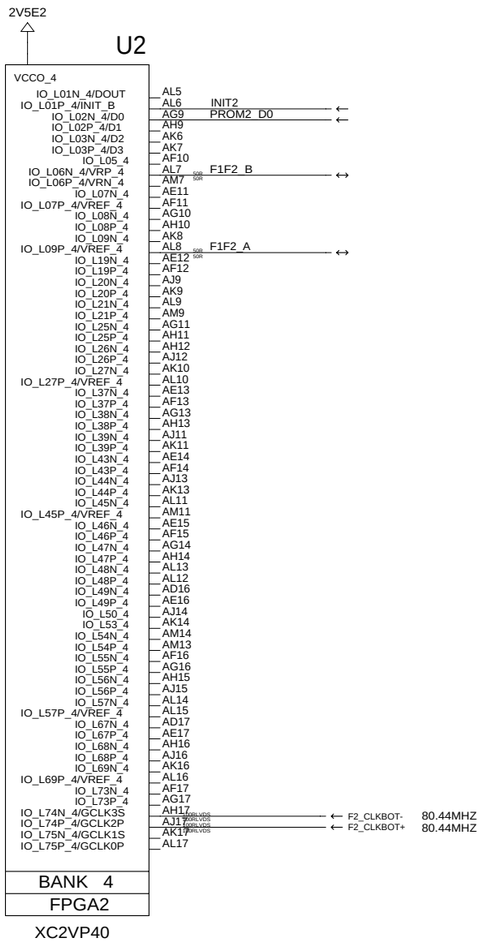
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA1 BANKS 2/3-TTCRX-USB-ETH		
Tue May 02 16:16:01 2006		
		SHEET 12 OF ??

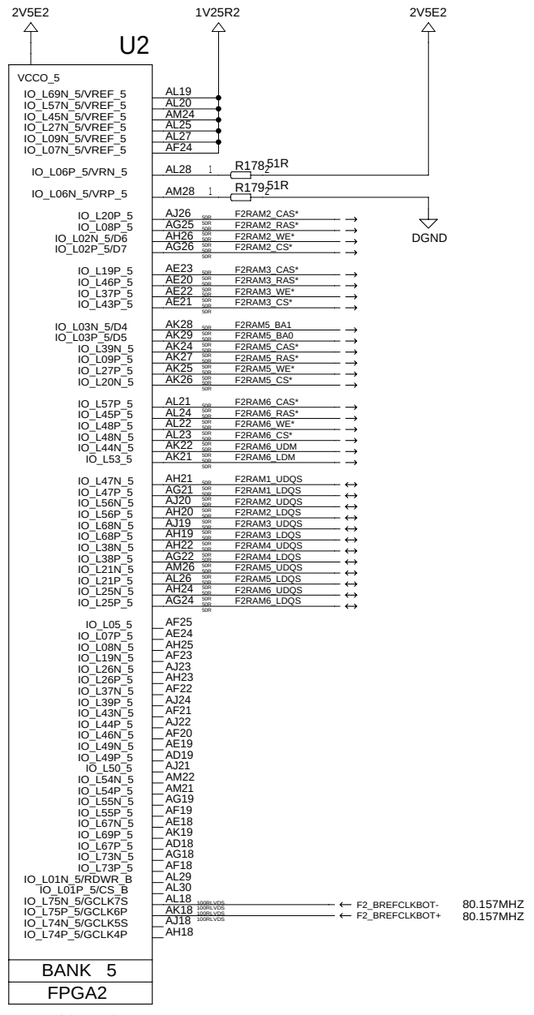

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XC2VP50
DEVELOPMENT
DRAWING
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA1 BANKS 6/7 (DDR SDRAM)
Tue May 02 16:16:02 2006
SHEET 13 OF ??







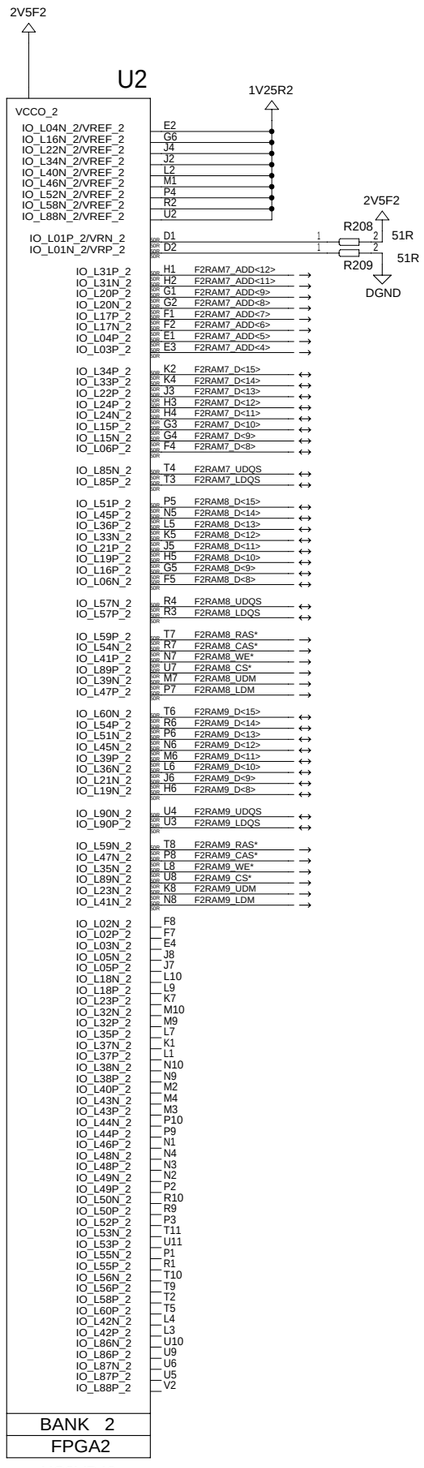


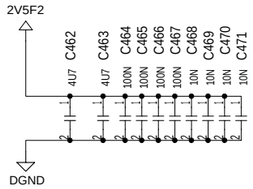


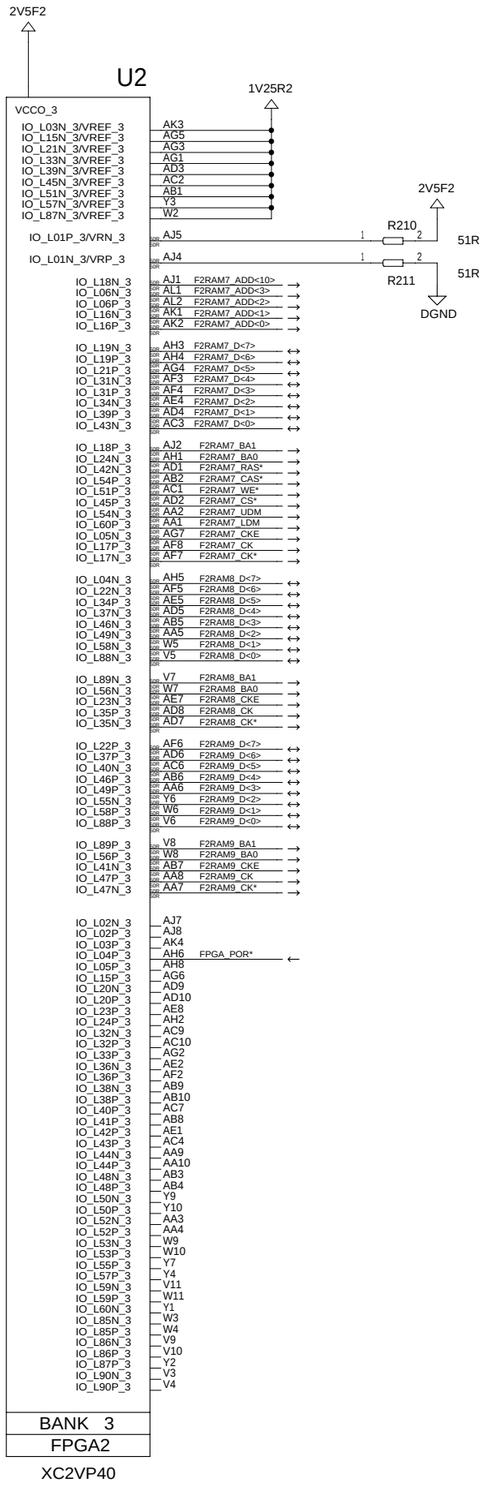
DEVELOPMENT

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UNIVERSITY OF CAMBRIDGE HEP		
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Tue May 02 16:16:03 2006		
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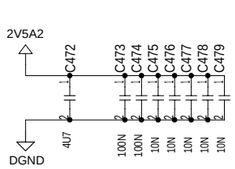


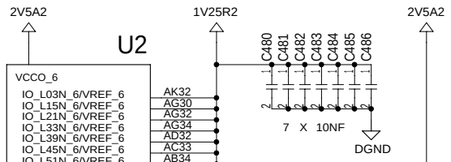


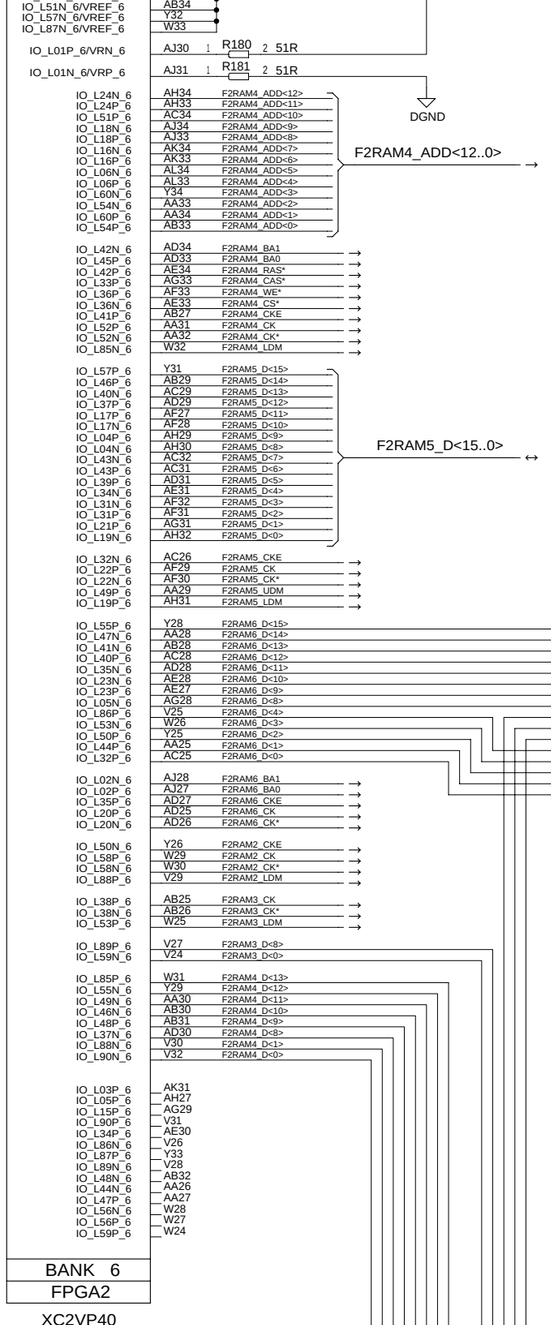
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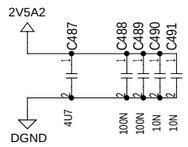
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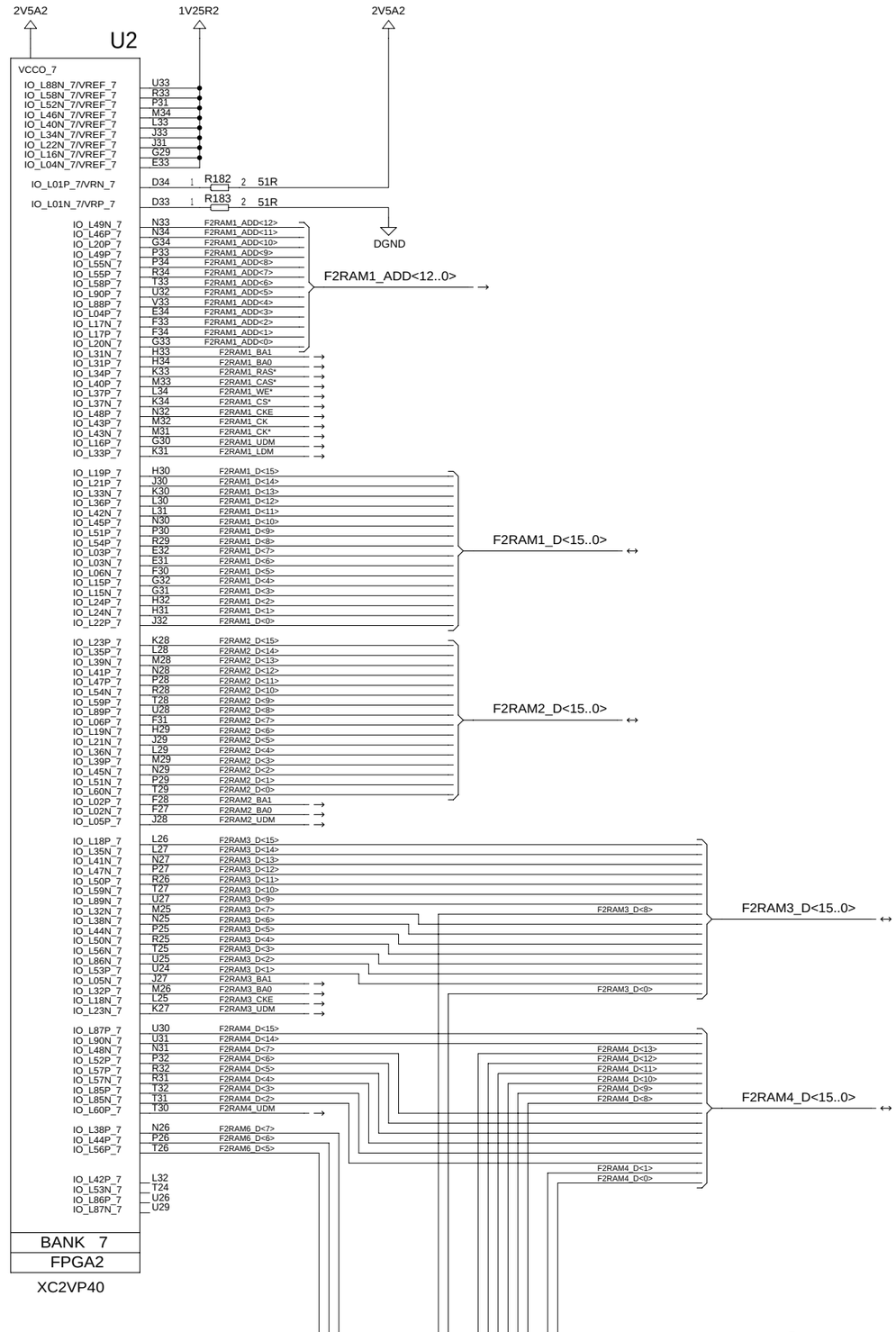
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DEVELOPMENT

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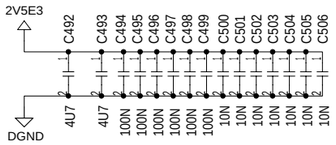
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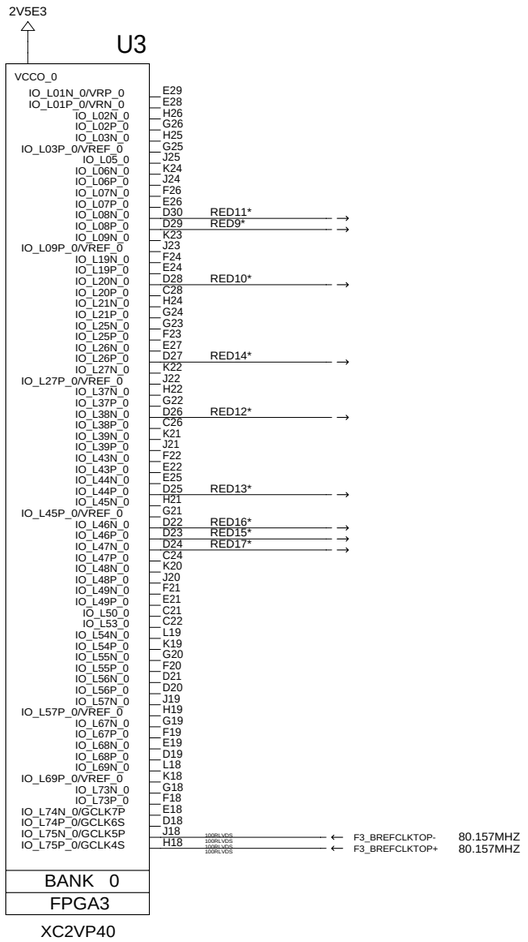
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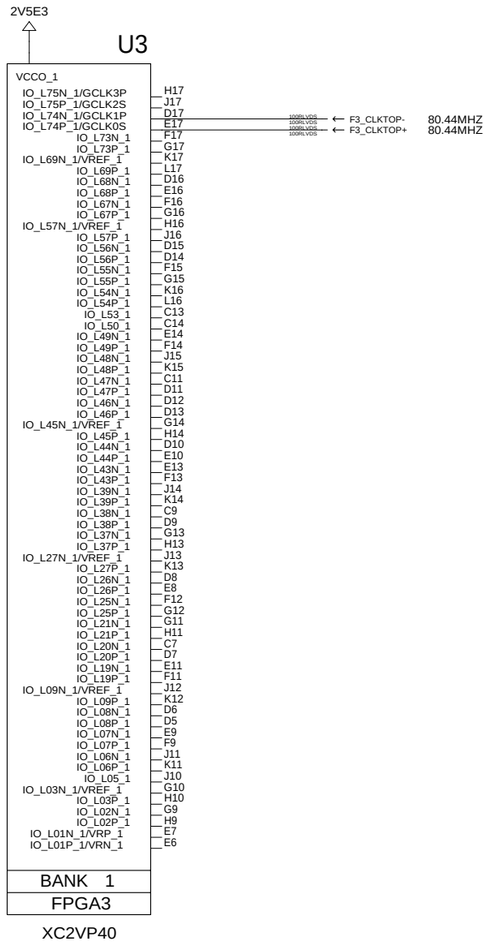
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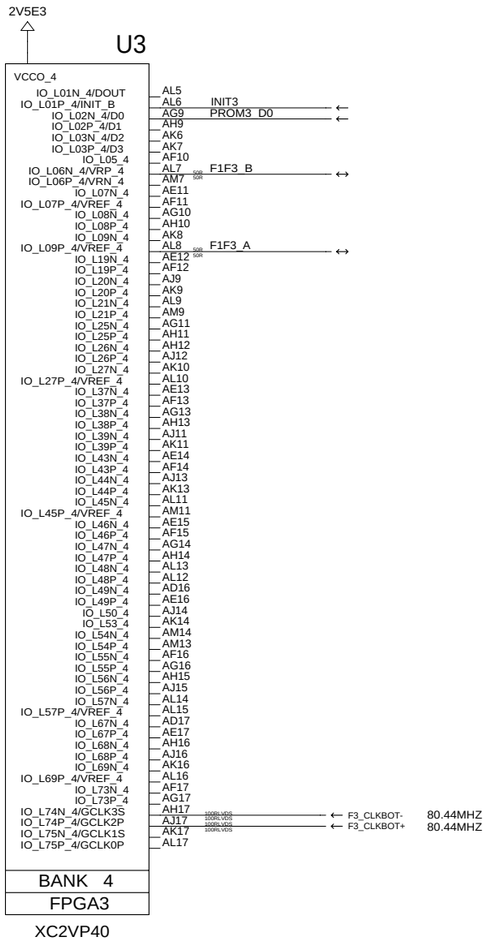
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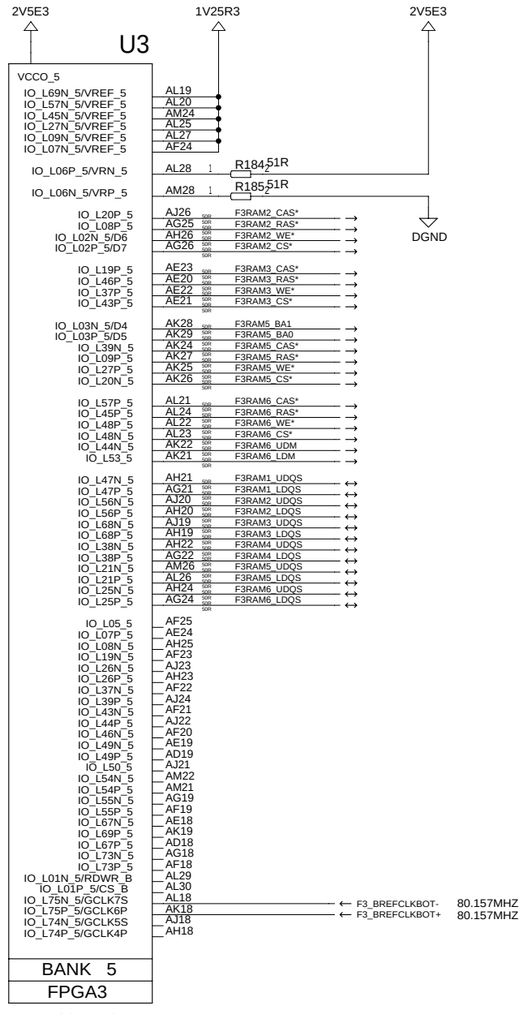
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DEVELOPMENT

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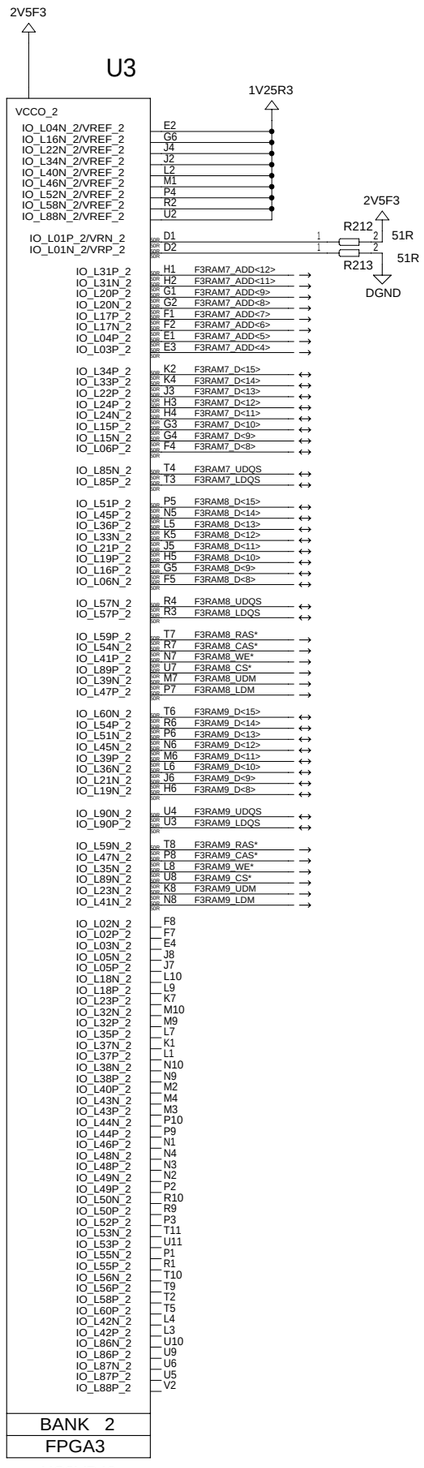
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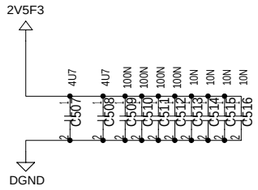
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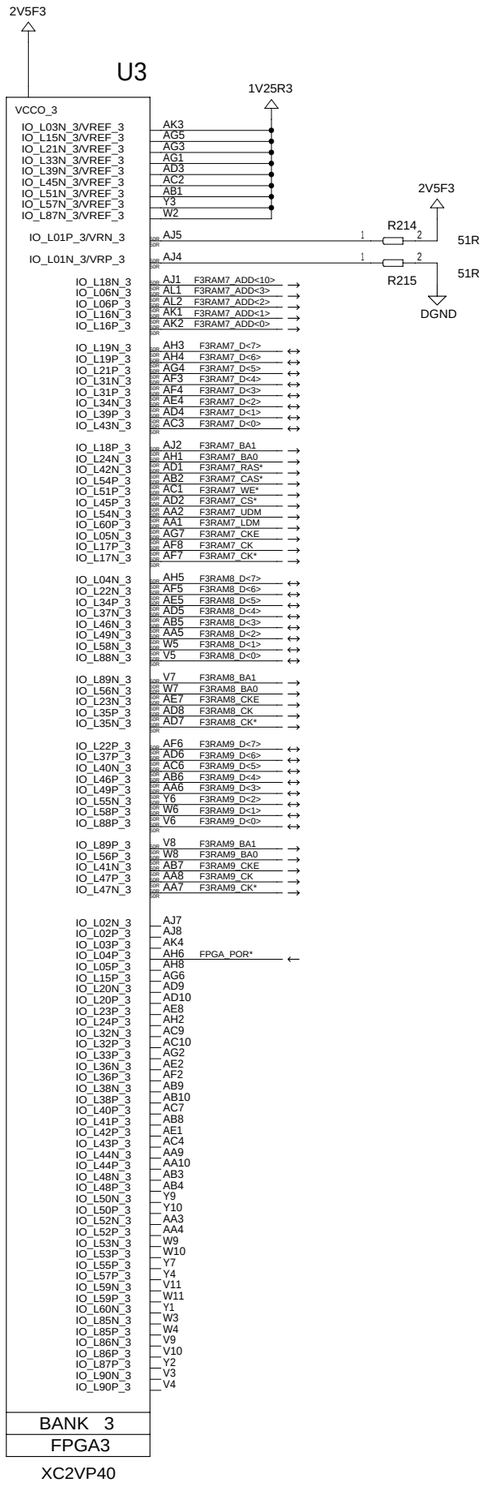
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SHEET 17 OF ??



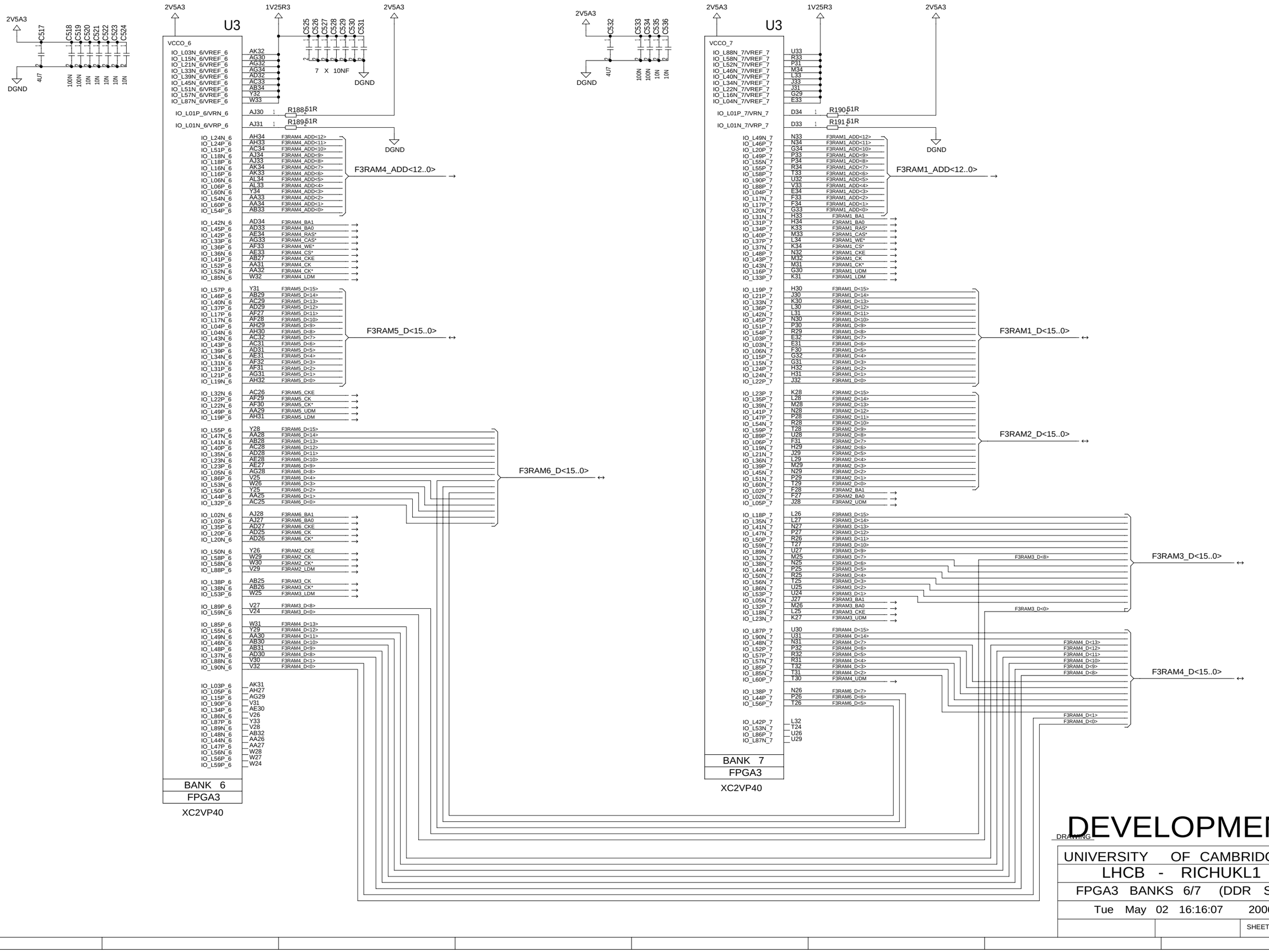


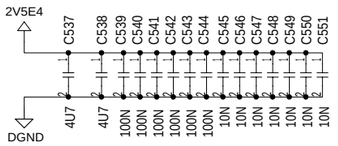


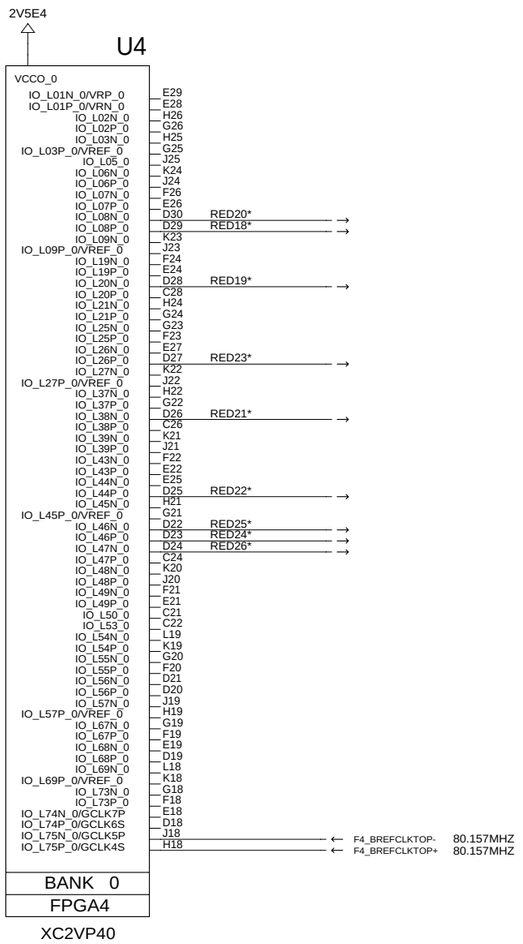
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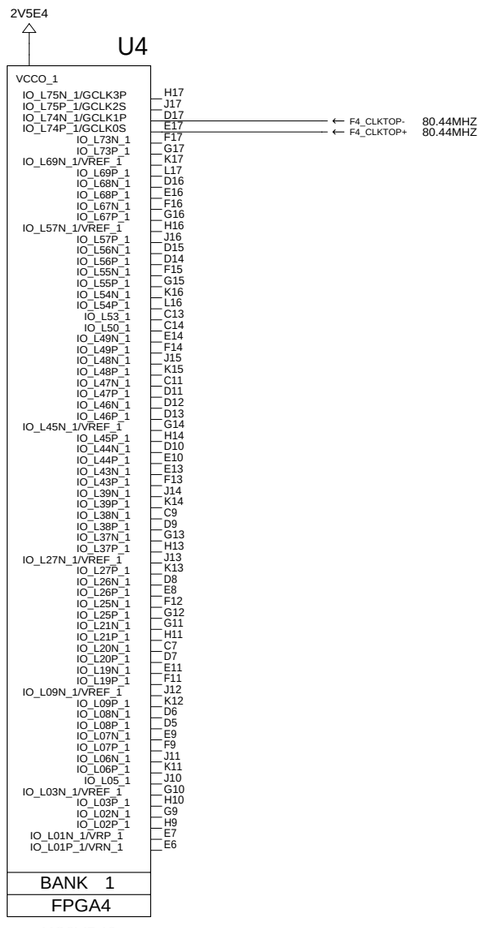
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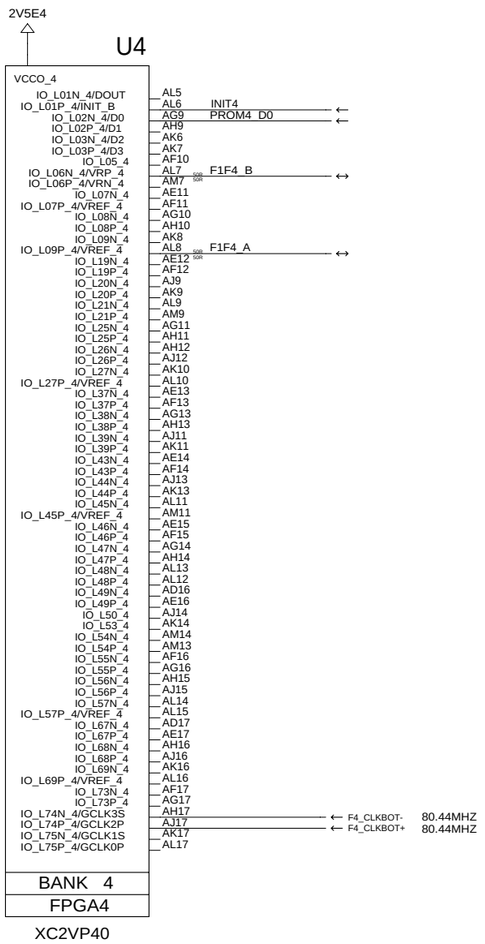
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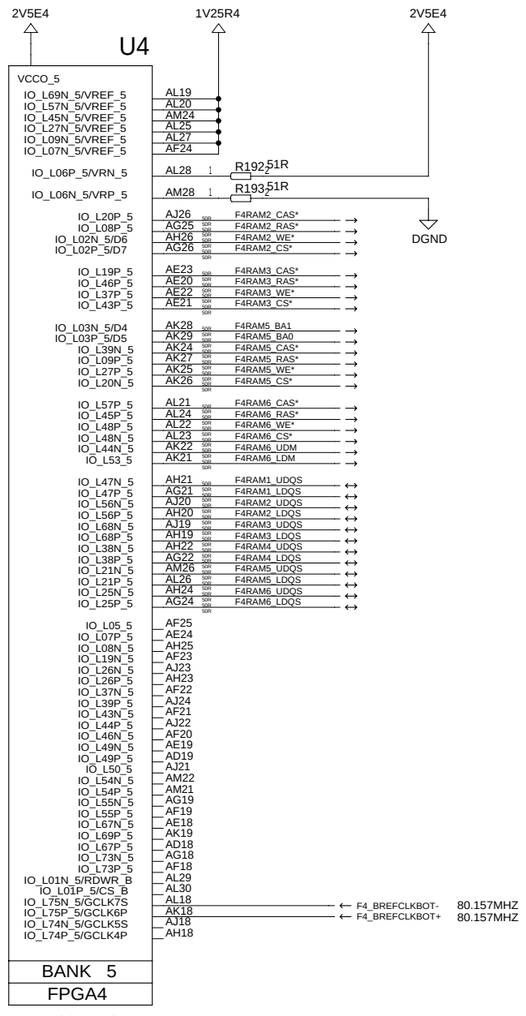

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10N
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DGND
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IO_L16N_7/VREF_7
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L33
J33
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D33
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R191 51R
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BANK 7
FPGA3
XC2VP40
DEVELOPMENT
DRAWING
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA3 BANKS 6/7 (DDR SDRAM)
Tue May 02 16:16:07 2006
SHEET 19 OF ??







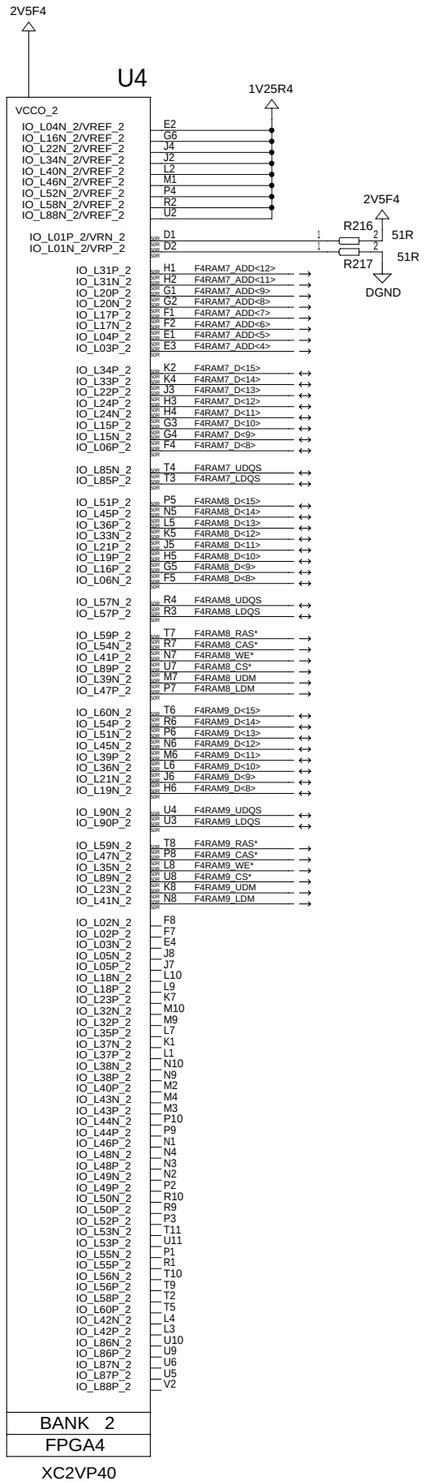


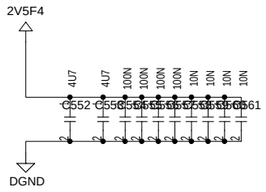


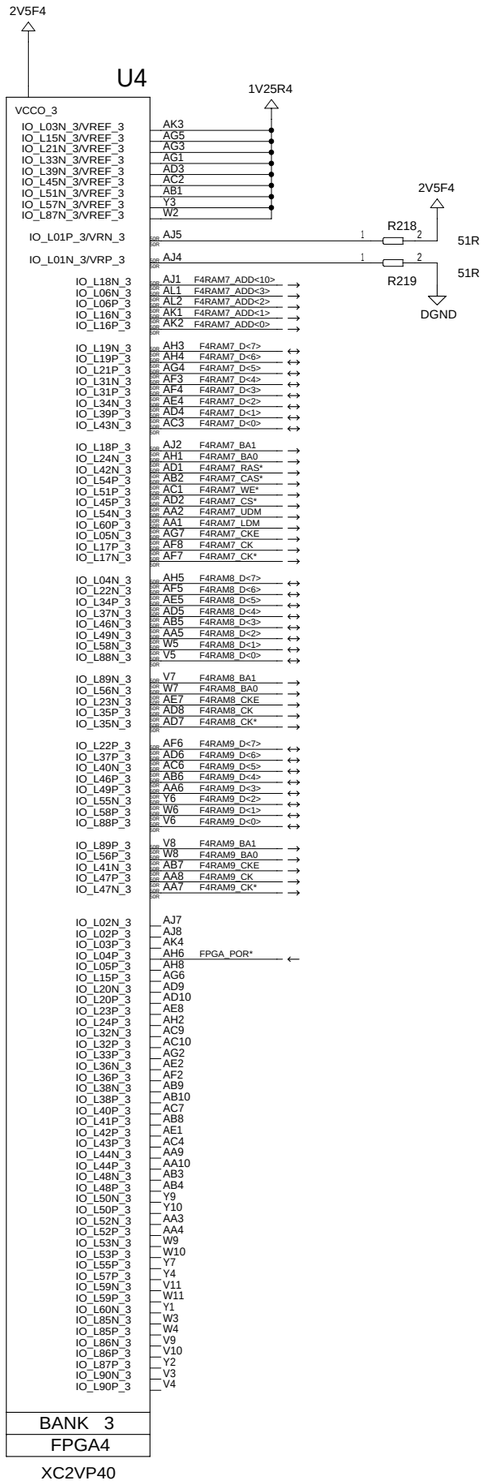
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UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA4 BANKS 0/1/4/5		
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		SHEET 20 OF ??



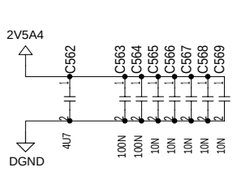


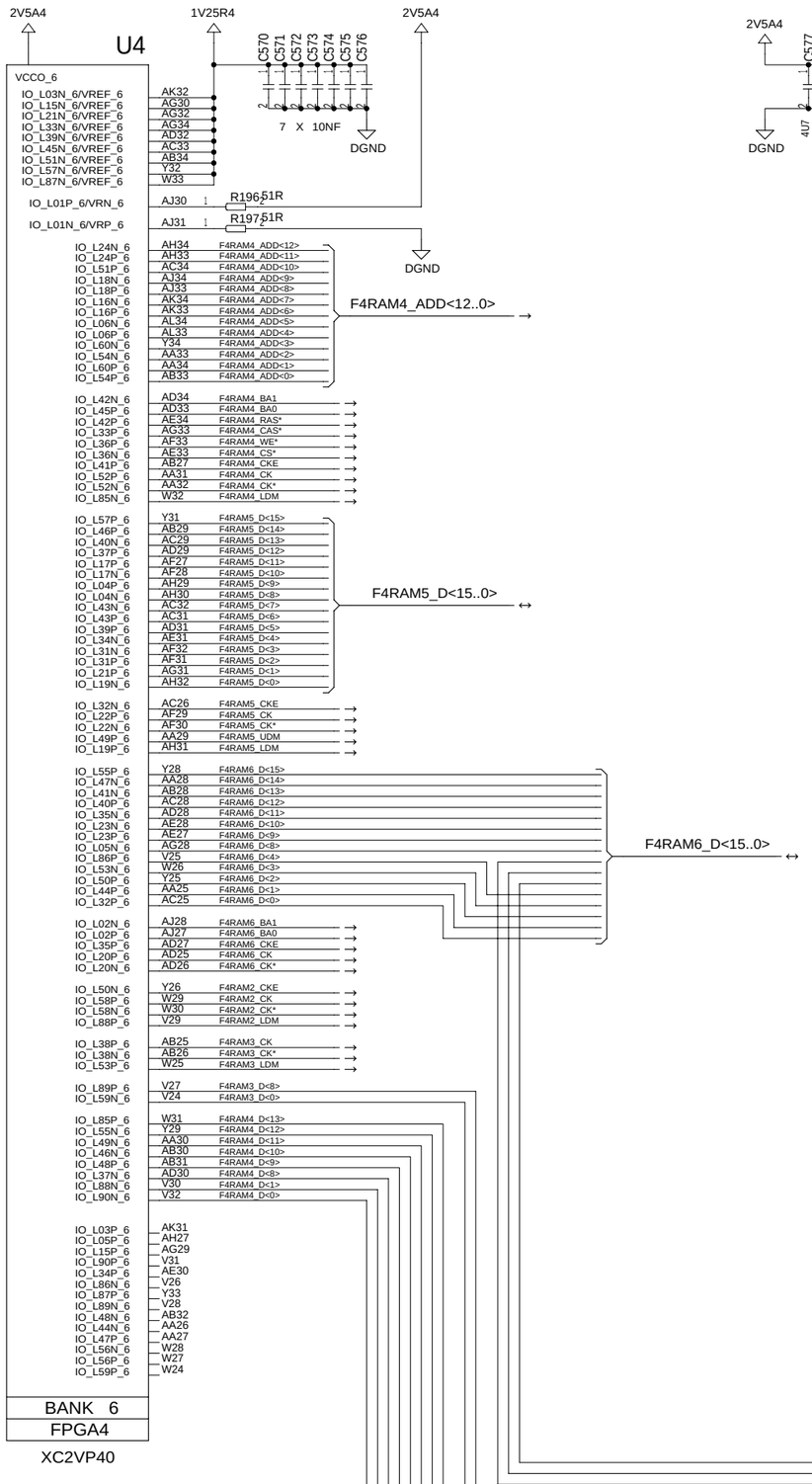


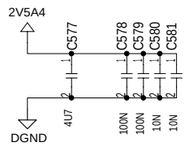
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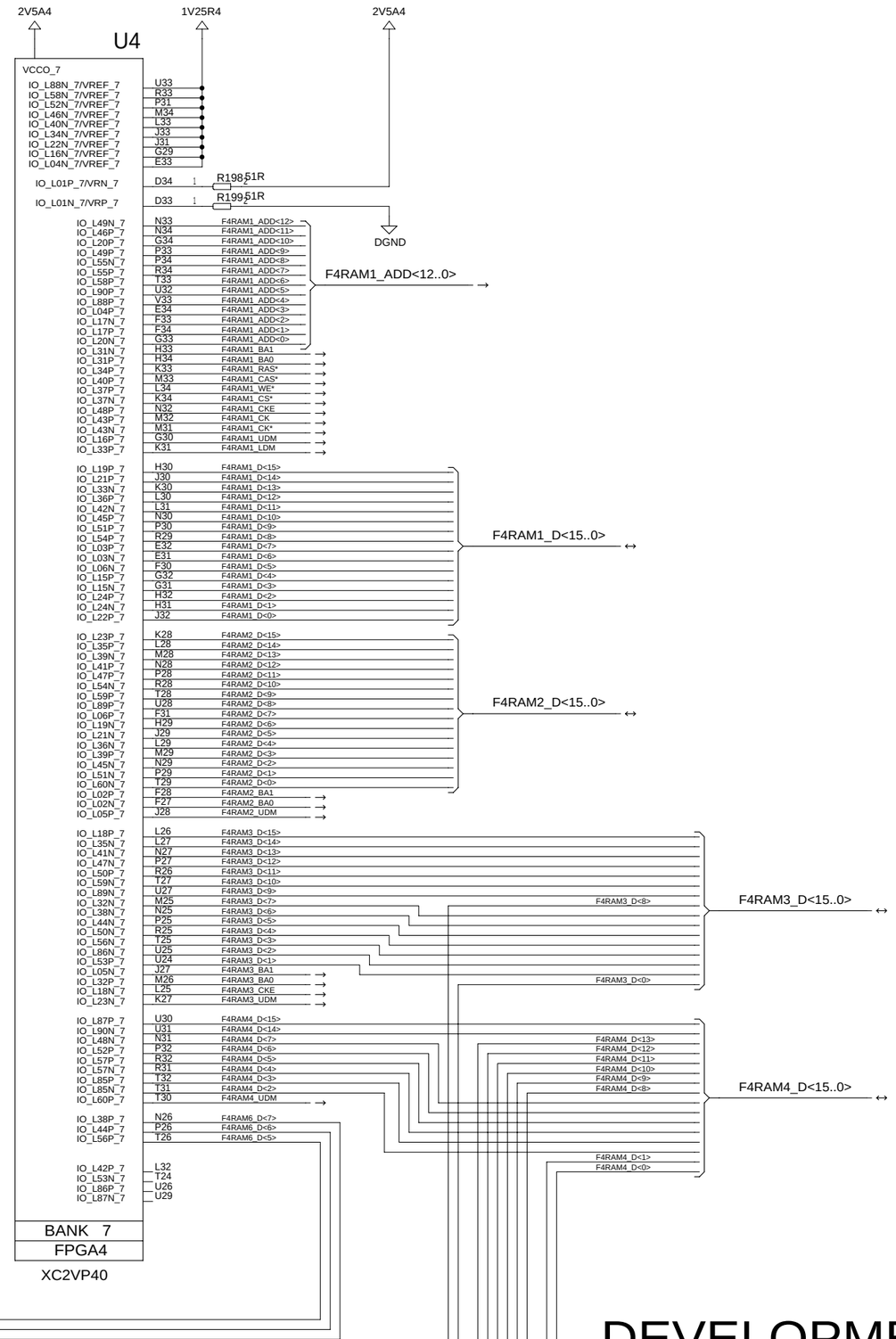
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UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA4 BANKS 2/3		
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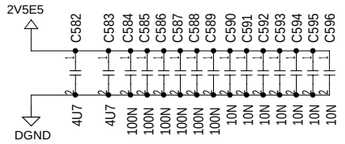


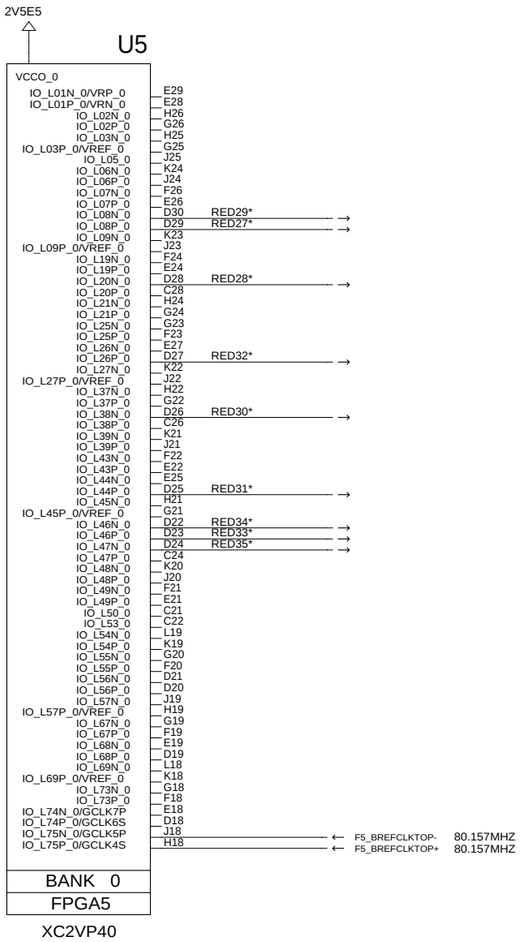


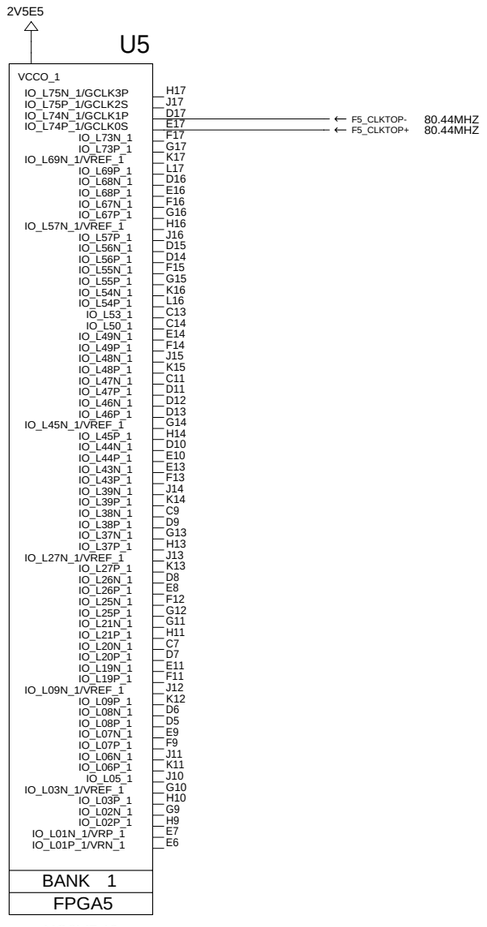
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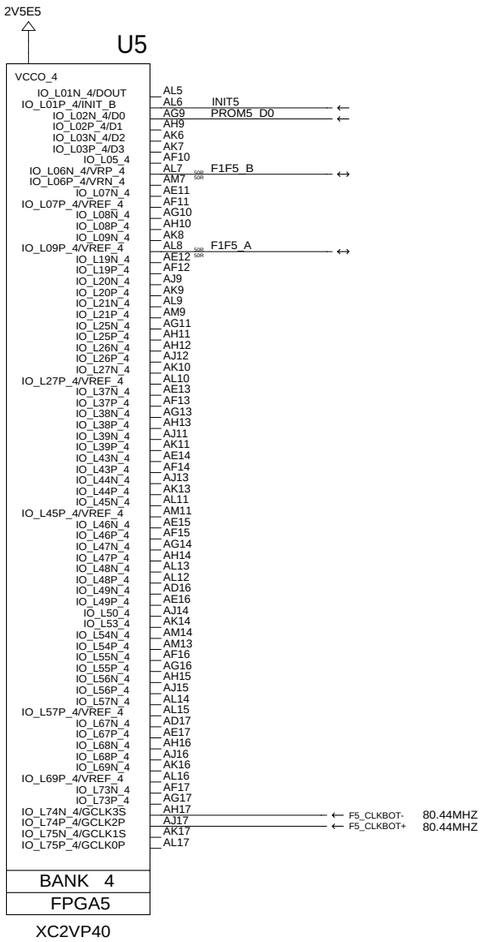
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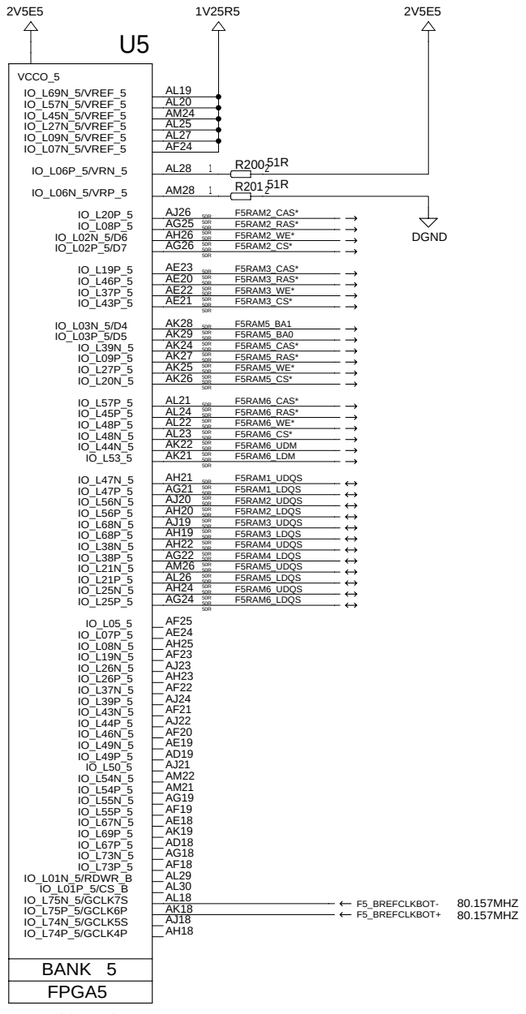
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LHCB - RICHUKL1		
FPGA4 BANKS 6/7 (DDR SDRAM)		
Tue May 02 16:16:09 2006		
		SHEET 22 OF ??











DEVELOPMENT

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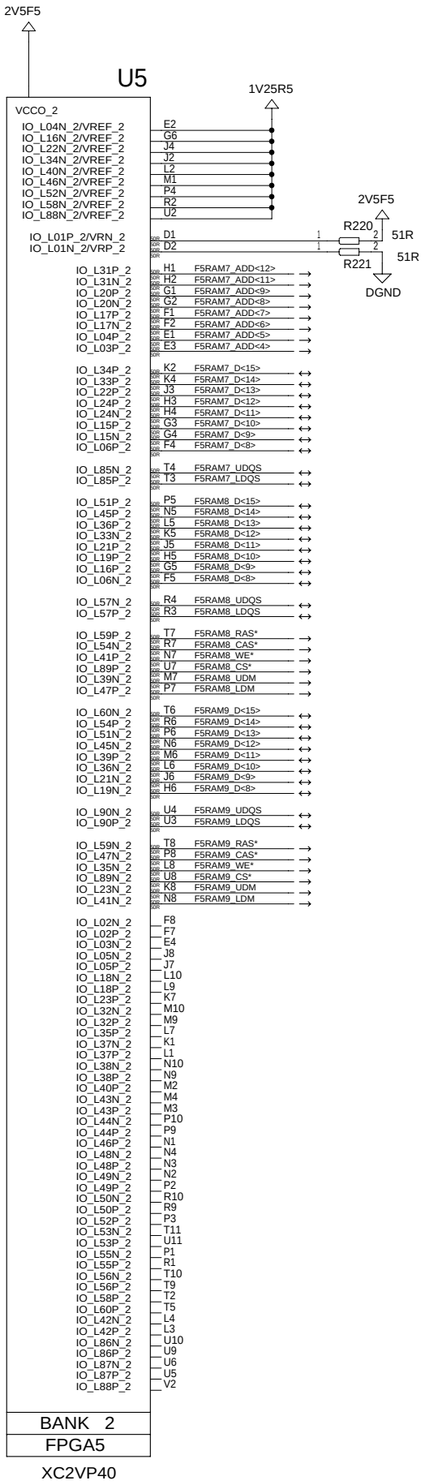
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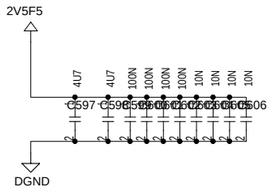
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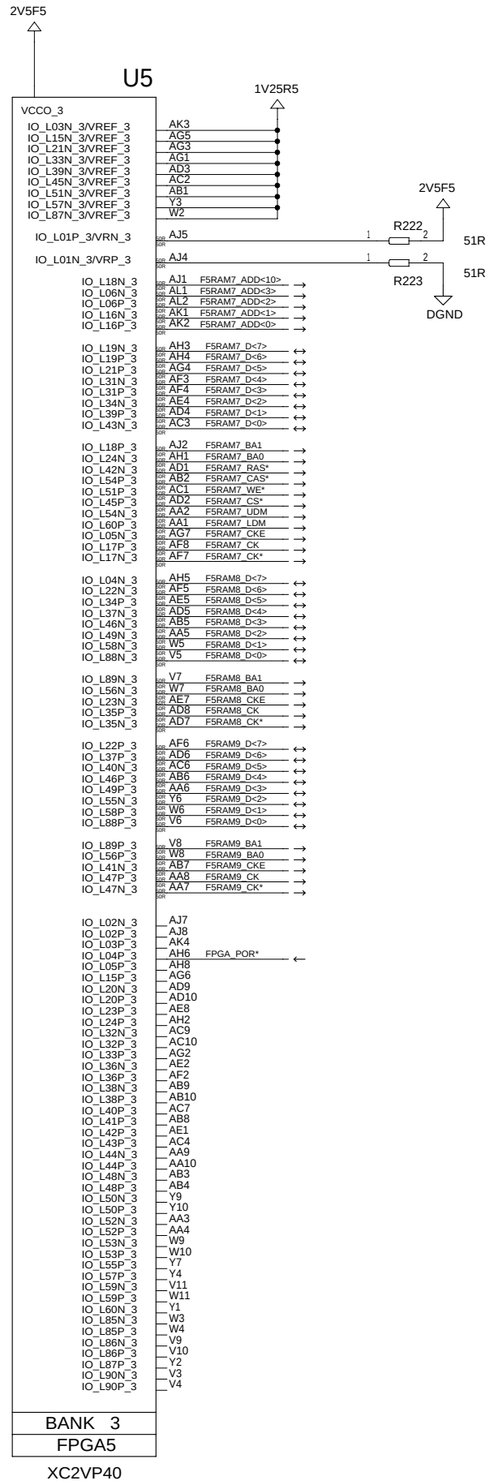
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SHEET 23 OF ??



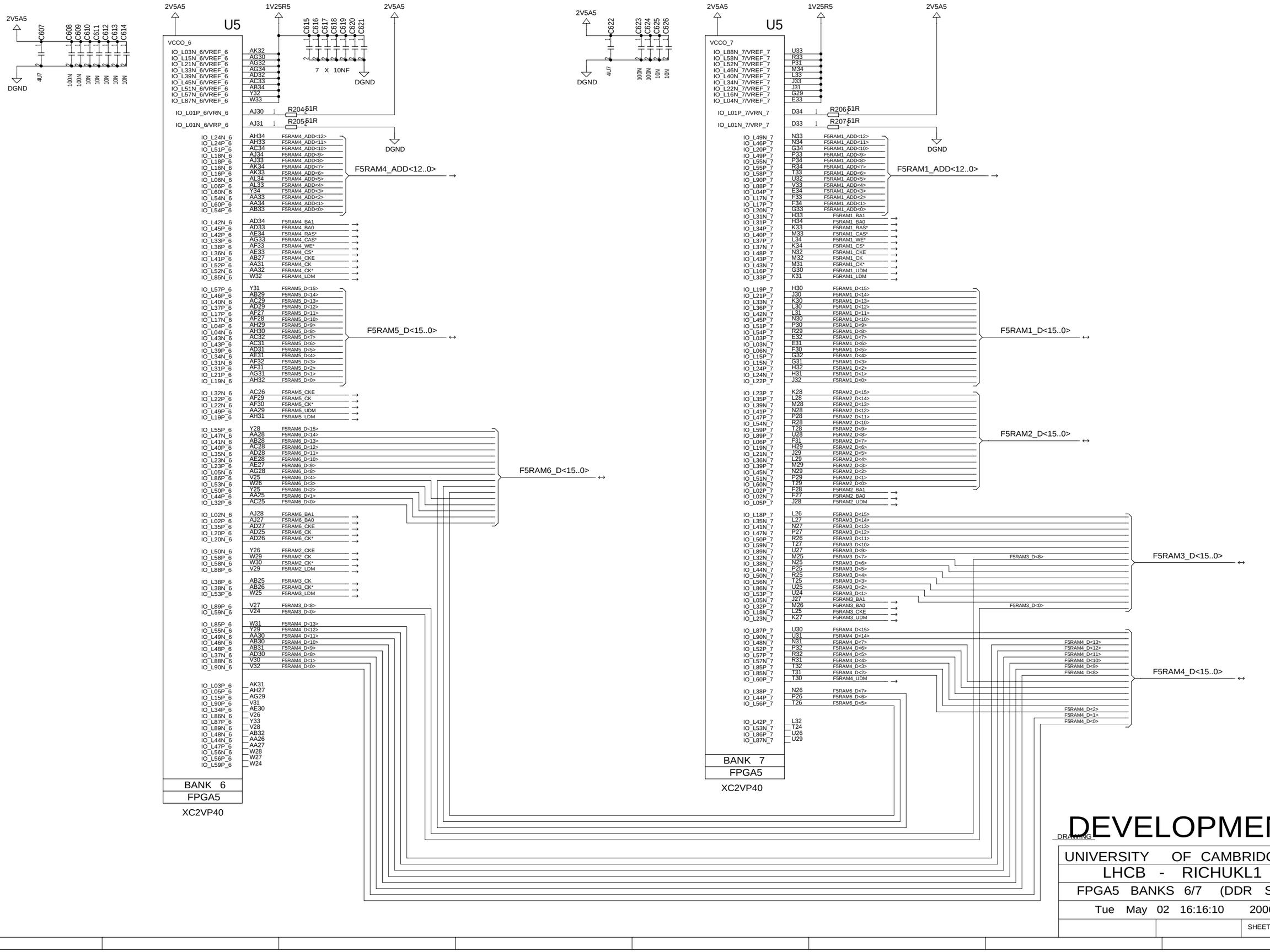


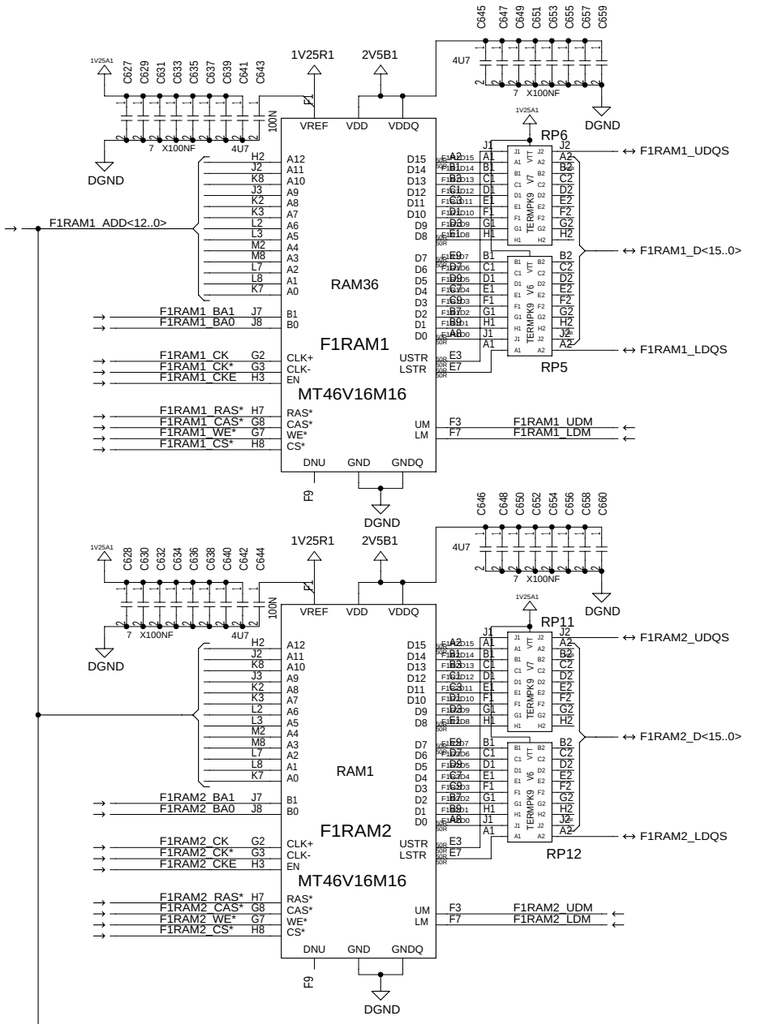


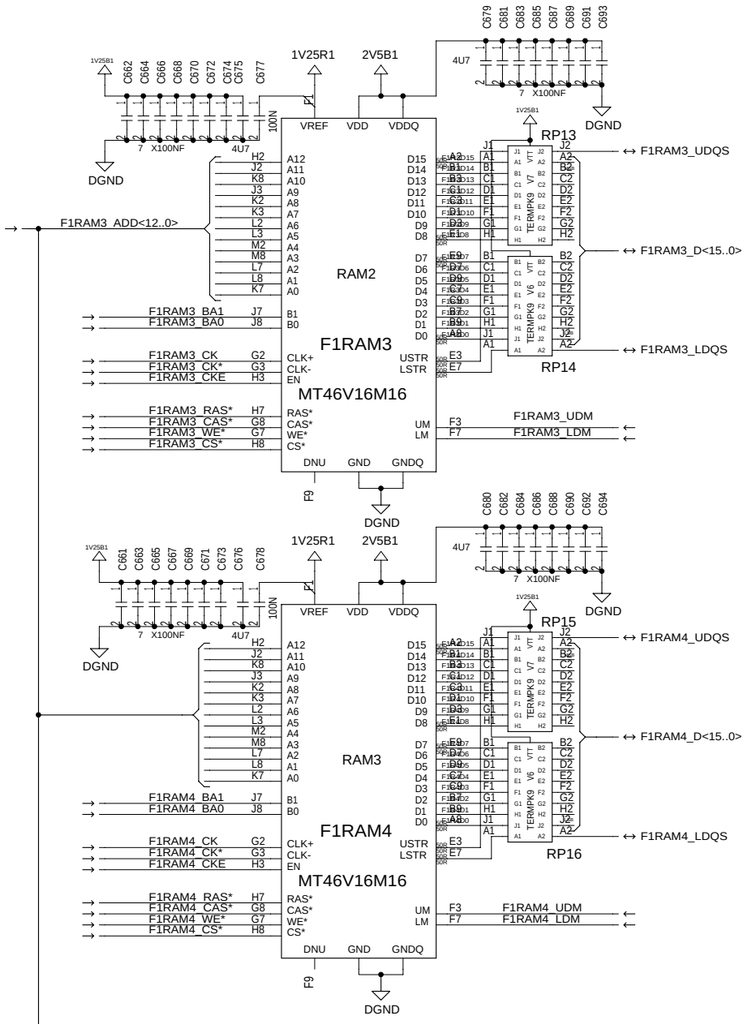
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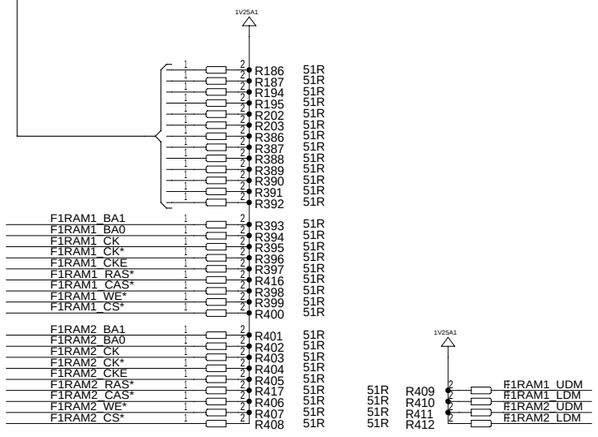
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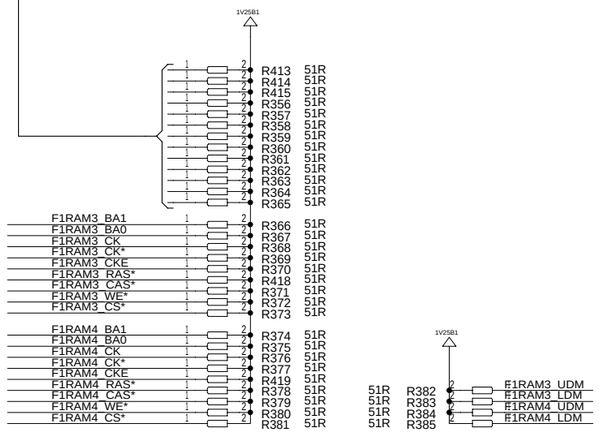
UNIVERSITY OF CAMBRIDGE HEP		
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FPGA5 BANKS 2/3		
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IO_L87N_6/VREF_6
1V25R5
C615
C616
C617
C618
C619
C620
C621
7 X 10NF
IO_L01P_6/VRN_6
IO_L01N_6/VRP_6
R204 51R
R205 51R
F5RAM4_ADD<12..0>
F5RAM4_BA1
F5RAM4_BA0
F5RAM4_RAS*
F5RAM4_CAS*
F5RAM4_WE*
F5RAM4_CS*
F5RAM4_CKE
F5RAM4_CK
F5RAM4_CK*
F5RAM4_LDM
F5RAM5_D<15..0>
F5RAM5_CKE
F5RAM5_CK
F5RAM5_CK*
F5RAM5_UDM
F5RAM5_LDM
F5RAM6_D<15..0>
F5RAM6_BA1
F5RAM6_BA0
F5RAM6_CKE
F5RAM6_CK
F5RAM6_CK*
F5RAM2_CKE
F5RAM2_CK
F5RAM2_CK*
F5RAM2_LDM
F5RAM3_CK
F5RAM3_CK*
F5RAM3_LDM
F5RAM3_D<8>
F5RAM3_D<0>
F5RAM4_D<13>
F5RAM4_D<12>
F5RAM4_D<11>
F5RAM4_D<10>
F5RAM4_D<9>
F5RAM4_D<8>
F5RAM4_D<1>
F5RAM4_D<0>
BANK 6
FPGA5
XC2VP40
2V5A5
C622
C623
C624
C625
C626
4U7
100N
100N
10N
10N
DGND
U5
VCCO_7
IO_L88N_7/VREF_7
IO_L58N_7/VREF_7
IO_L52N_7/VREF_7
IO_L46N_7/VREF_7
IO_L40N_7/VREF_7
IO_L34N_7/VREF_7
IO_L22N_7/VREF_7
IO_L16N_7/VREF_7
IO_L04N_7/VREF_7
IO_L01P_7/VRN_7
IO_L01N_7/VRP_7
R206 51R
R207 51R
F5RAM1_ADD<12..0>
F5RAM1_BA1
F5RAM1_BA0
F5RAM1_RAS*
F5RAM1_CAS*
F5RAM1_WE*
F5RAM1_CS*
F5RAM1_CKE
F5RAM1_CK
F5RAM1_CK*
F5RAM1_UDM
F5RAM1_LDM
F5RAM1_D<15..0>
F5RAM2_D<15..0>
F5RAM2_D<4>
F5RAM2_D<3>
F5RAM2_D<2>
F5RAM2_D<1>
F5RAM2_D<0>
F5RAM2_BA1
F5RAM2_BA0
F5RAM2_UDM
F5RAM3_D<15..0>
F5RAM3_D<14>
F5RAM3_D<13>
F5RAM3_D<12>
F5RAM3_D<11>
F5RAM3_D<10>
F5RAM3_D<9>
F5RAM3_D<7>
F5RAM3_D<6>
F5RAM3_D<5>
F5RAM3_D<4>
F5RAM3_D<3>
F5RAM3_D<2>
F5RAM3_D<1>
F5RAM3_BA1
F5RAM3_BA0
F5RAM3_CKE
F5RAM3_UDM
F5RAM4_D<15..0>
F5RAM4_D<14>
F5RAM4_D<7>
F5RAM4_D<6>
F5RAM4_D<5>
F5RAM4_D<4>
F5RAM4_D<3>
F5RAM4_D<2>
F5RAM4_UDM
F5RAM6_D<7>
F5RAM6_D<6>
F5RAM6_D<5>
BANK 7
FPGA5
XC2VP40
DEVELOPMENT
DRAWING
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA5 BANKS 6/7 (DDR SDRAM)
Tue May 02 16:16:10 2006
SHEET 25 OF ??









1V25

5F1R

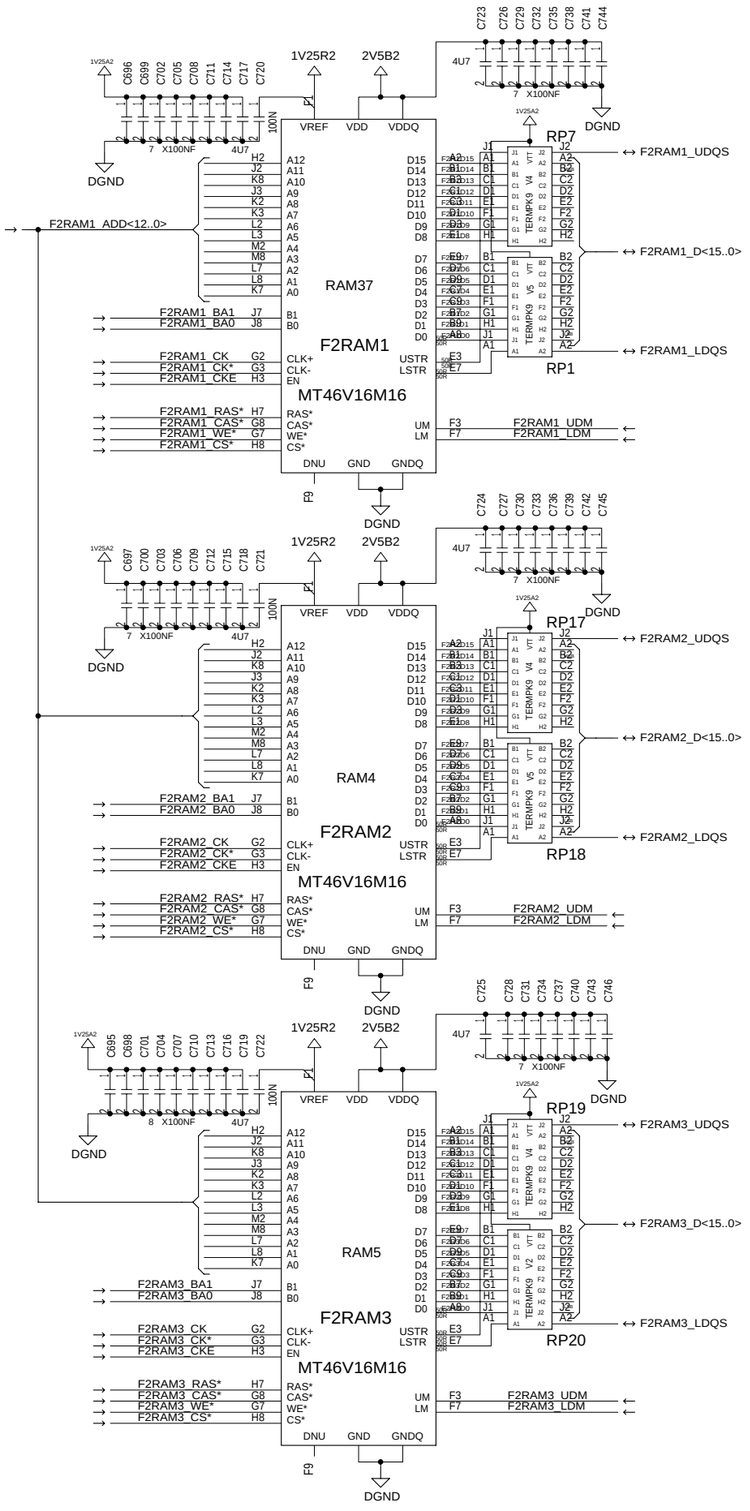
25R

X 9

DEVELOPMENT

DRAWING

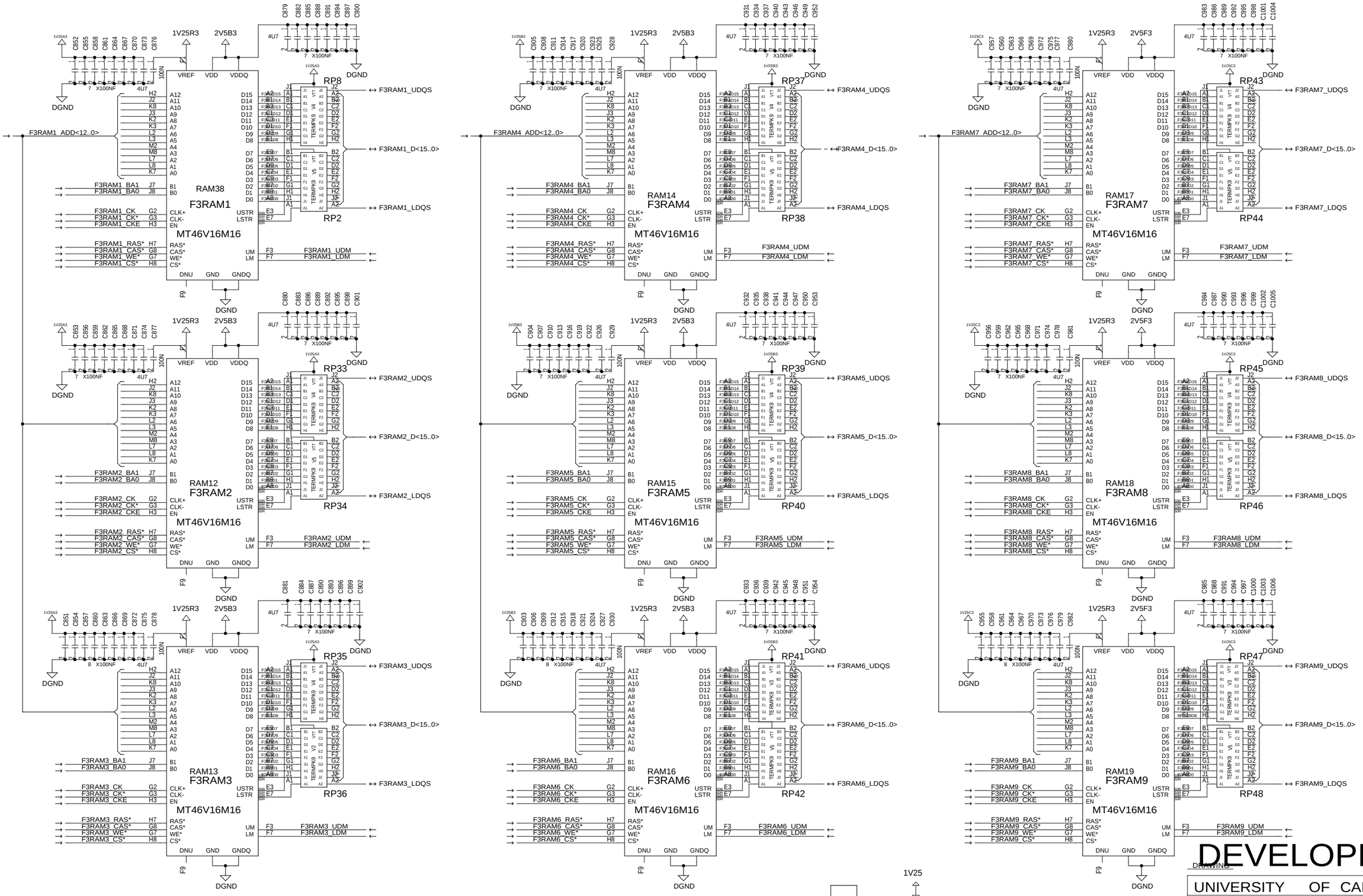
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA1 RAMS 1 - 4		
Tue May 02 16:16:12 2006		
		SHEET 26 OF ??

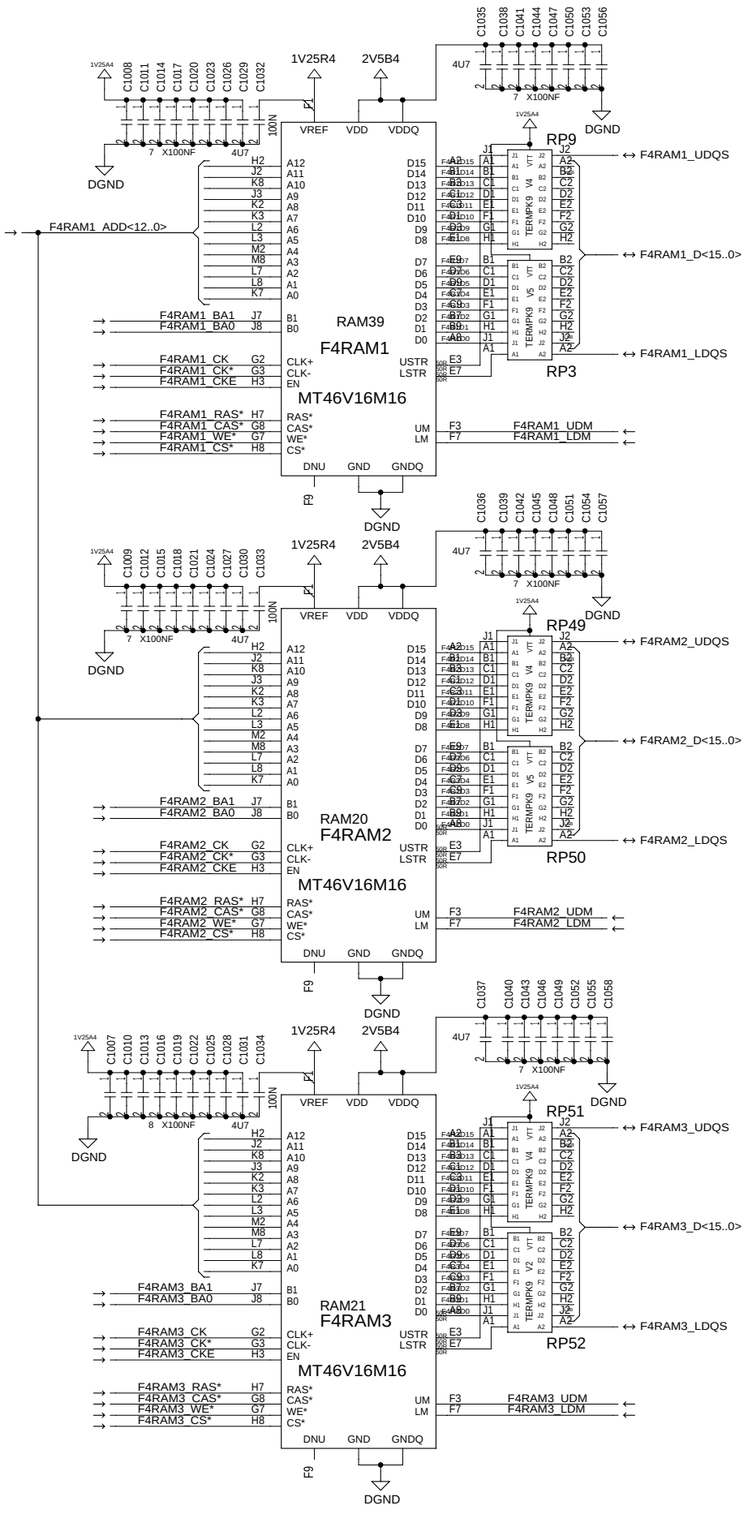


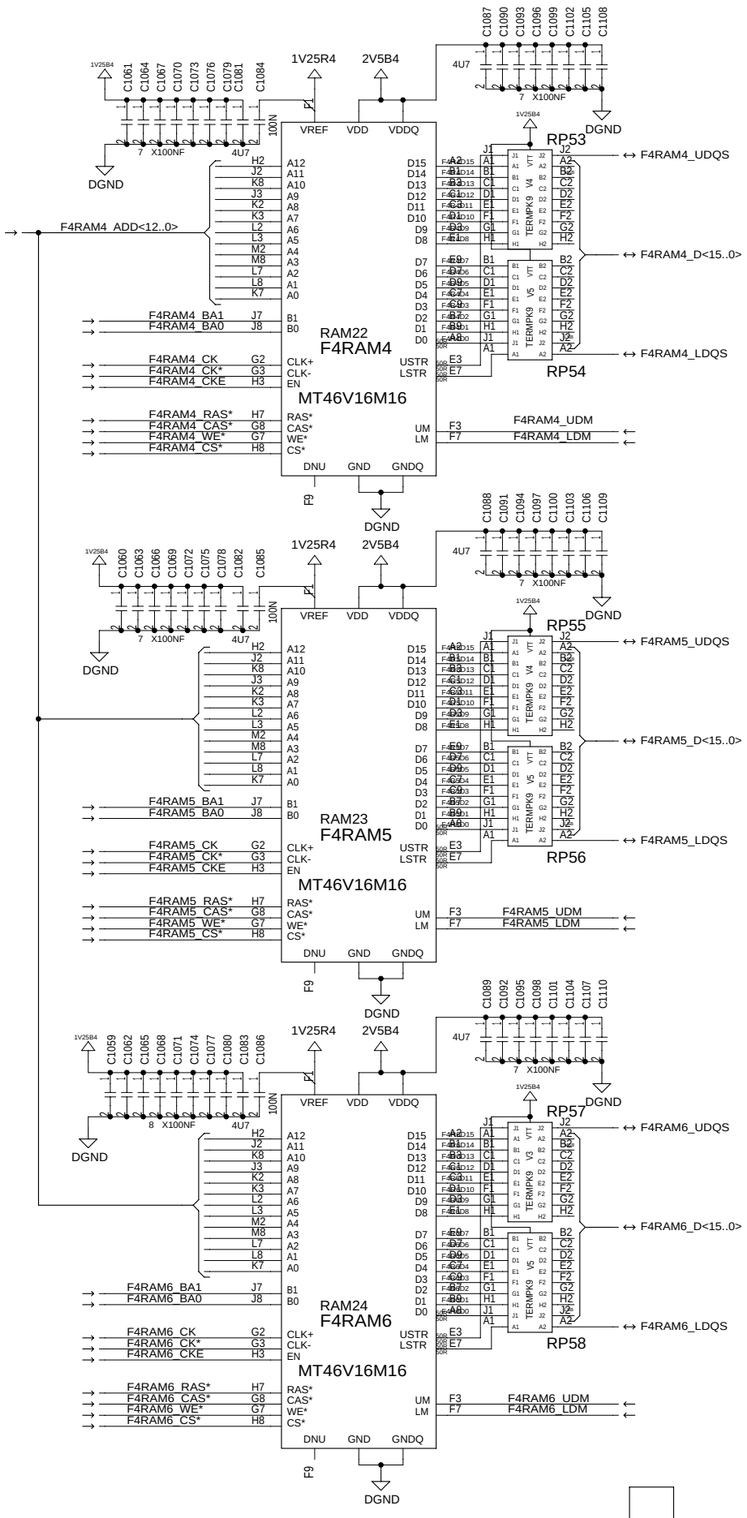
DEVELOPMENT

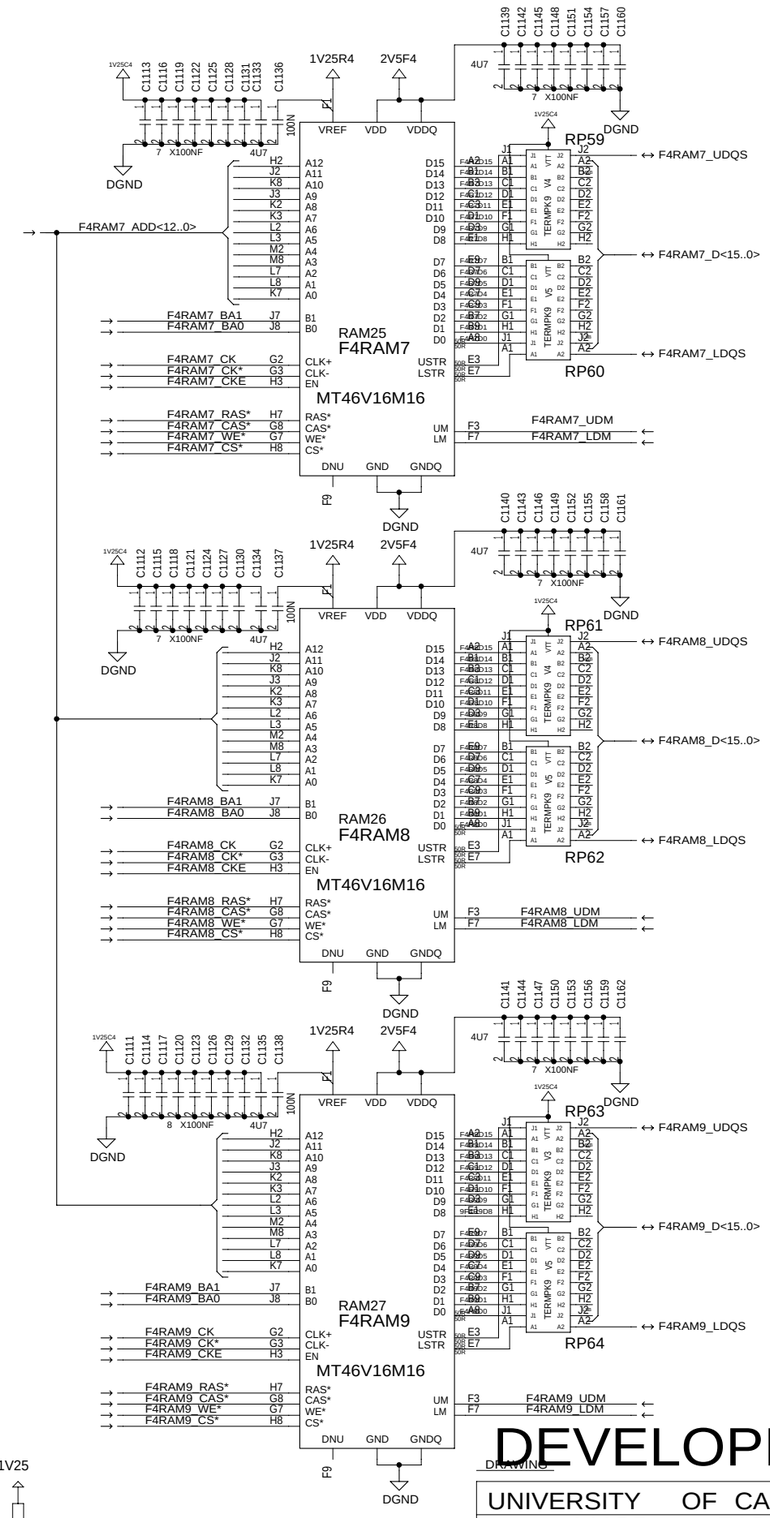
DRAWING

UNIVERSITY OF CAMBRIDGE HEP	
LHCB - RICHUKL1	
FPGA2 RAMS 1 - 9	
Tue May 02 16:16:14 2006	
	SHEET 27 OF ??


RAM38
F3RAM1
MT46V16M16
RP8
RP2
F3RAM1_ADD<12..0>
F3RAM1_BA1
F3RAM1_BA0
F3RAM1_CK
F3RAM1_CK*
F3RAM1_CKE
F3RAM1_RAS*
F3RAM1_CAS*
F3RAM1_WE*
F3RAM1_CS*
F3RAM1_UDQS
F3RAM1_D<15..0>
F3RAM1_LDQS
F3RAM1_UDM
F3RAM1_LDM
RAM12
F3RAM2
RP33
RP34
F3RAM2_ADD<12..0>
F3RAM2_UDQS
F3RAM2_D<15..0>
F3RAM2_LDQS
F3RAM2_UDM
F3RAM2_LDM
RAM13
F3RAM3
RP35
RP36
F3RAM3_ADD<12..0>
F3RAM3_UDQS
F3RAM3_D<15..0>
F3RAM3_LDQS
F3RAM3_UDM
F3RAM3_LDM
RAM14
F3RAM4
RP37
RP38
F3RAM4_ADD<12..0>
F3RAM4_UDQS
F3RAM4_D<15..0>
F3RAM4_LDQS
F3RAM4_UDM
F3RAM4_LDM
RAM15
F3RAM5
RP39
RP40
F3RAM5_ADD<12..0>
F3RAM5_UDQS
F3RAM5_D<15..0>
F3RAM5_LDQS
F3RAM5_UDM
F3RAM5_LDM
RAM16
F3RAM6
RP41
RP42
F3RAM6_ADD<12..0>
F3RAM6_UDQS
F3RAM6_D<15..0>
F3RAM6_LDQS
F3RAM6_UDM
F3RAM6_LDM
RAM17
F3RAM7
RP43
RP44
F3RAM7_ADD<12..0>
F3RAM7_UDQS
F3RAM7_D<15..0>
F3RAM7_LDQS
F3RAM7_UDM
F3RAM7_LDM
RAM18
F3RAM8
RP45
RP46
F3RAM8_ADD<12..0>
F3RAM8_UDQS
F3RAM8_D<15..0>
F3RAM8_LDQS
F3RAM8_UDM
F3RAM8_LDM
RAM19
F3RAM9
RP47
RP48
F3RAM9_ADD<12..0>
F3RAM9_UDQS
F3RAM9_D<15..0>
F3RAM9_LDQS
F3RAM9_UDM
F3RAM9_LDM
MT46V16M16
1V25R3
2V5B3
2V5F3
4U7
X100NF
100N
DGND
VREF
VDD
VDDQ
DNU
GND
GNDQ
1V25
X 9
DEVELOPMENT
DRAWING
UNIVERSITY OF CAMBRIDGE HEP
LHCB - RICHUKL1
FPGA3 RAMS 1 - 9
Tue May 02 16:16:16 2006
SHEET 28 OF ??







1V25

X 9

DEVELOPMENT

DRAWING

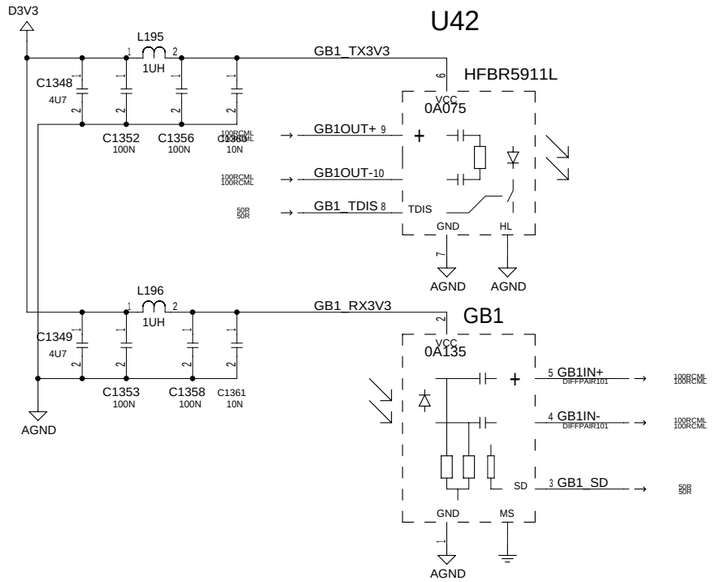
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA4 RAMS 1 - 9		
Tue May 02 16:16:18 2006		
		SHEET 29 OF ??

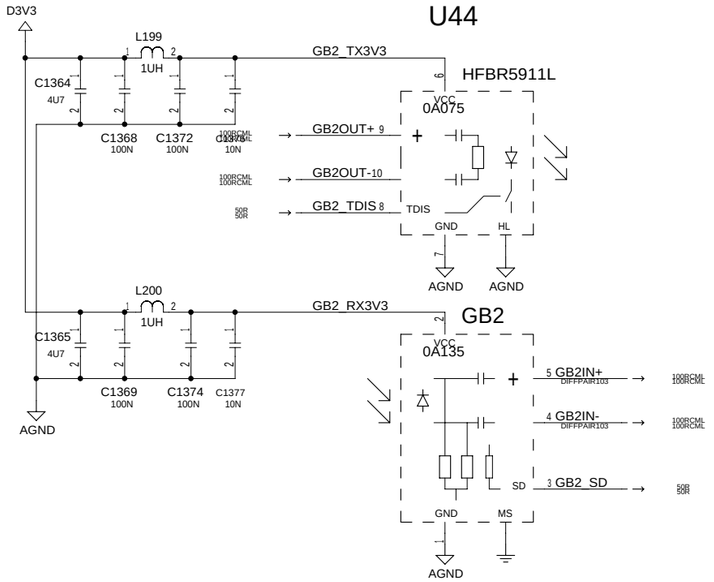
RAM40 F5RAM1 MT46V16M16 RP10 RP4
RAM30 F5RAM4 MT46V16M16 RP69 RP70
RAM33 F5RAM7 MT46V16M16 RP75 RP76
RAM28 F5RAM2 MT46V16M16 RP65 RP66
RAM31 F5RAM5 MT46V16M16 RP71 RP72
RAM34 F5RAM8 MT46V16M16 RP77 RP78
RAM29 F5RAM3 MT46V16M16 RP67 RP68
RAM32 F5RAM6 MT46V16M16 RP73 RP74
RAM35 F5RAM9 MT46V16M16 RP79 RP80
1V25R5 2V5B5 2V5F5 VREF VDD VDDQ DNU GND GNDQ
4U7 X100NF 8 X100NF 100N
F5RAM1_ADD<12..0> F5RAM4_ADD<12..0> F5RAM7_ADD<12..0>
F5RAM2_ADD<12..0> F5RAM5_ADD<12..0> F5RAM8_ADD<12..0>
F5RAM3_ADD<12..0> F5RAM6_ADD<12..0> F5RAM9_ADD<12..0>
F5RAM1_BA1 F5RAM1_BA0 F5RAM1_CK F5RAM1_CK* F5RAM1_CKE
F5RAM1_RAS* F5RAM1_CAS* F5RAM1_WE* F5RAM1_CS*
F5RAM1_UDQS F5RAM1_D<15..0> F5RAM1_LDQS F5RAM1_UDM F5RAM1_LDM
F5RAM4_BA1 F5RAM4_BA0 F5RAM4_CK F5RAM4_CK* F5RAM4_CKE
F5RAM4_RAS* F5RAM4_CAS* F5RAM4_WE* F5RAM4_CS*
F5RAM4_UDQS F5RAM4_D<15..0> F5RAM4_LDQS F5RAM4_UDM F5RAM4_LDM
F5RAM7_BA1 F5RAM7_BA0 F5RAM7_CK F5RAM7_CK* F5RAM7_CKE
F5RAM7_RAS* F5RAM7_CAS* F5RAM7_WE* F5RAM7_CS*
F5RAM7_UDQS F5RAM7_D<15..0> F5RAM7_LDQS F5RAM7_UDM F5RAM7_LDM
F5RAM2_BA1 F5RAM2_BA0 F5RAM2_CK F5RAM2_CK* F5RAM2_CKE
F5RAM2_RAS* F5RAM2_CAS* F5RAM2_WE* F5RAM2_CS*
F5RAM2_UDQS F5RAM2_D<15..0> F5RAM2_LDQS F5RAM2_UDM F5RAM2_LDM
F5RAM5_BA1 F5RAM5_BA0 F5RAM5_CK F5RAM5_CK* F5RAM5_CKE
F5RAM5_RAS* F5RAM5_CAS* F5RAM5_WE* F5RAM5_CS*
F5RAM5_UDQS F5RAM5_D<15..0> F5RAM5_LDQS F5RAM5_UDM F5RAM5_LDM
F5RAM8_BA1 F5RAM8_BA0 F5RAM8_CK F5RAM8_CK* F5RAM8_CKE
F5RAM8_RAS* F5RAM8_CAS* F5RAM8_WE* F5RAM8_CS*
F5RAM8_UDQS F5RAM8_D<15..0> F5RAM8_LDQS F5RAM8_UDM F5RAM8_LDM
F5RAM3_BA1 F5RAM3_BA0 F5RAM3_CK F5RAM3_CK* F5RAM3_CKE
F5RAM3_RAS* F5RAM3_CAS* F5RAM3_WE* F5RAM3_CS*
F5RAM3_UDQS F5RAM3_D<15..0> F5RAM3_LDQS F5RAM3_UDM F5RAM3_LDM
F5RAM6_BA1 F5RAM6_BA0 F5RAM6_CK F5RAM6_CK* F5RAM6_CKE
F5RAM6_RAS* F5RAM6_CAS* F5RAM6_WE* F5RAM6_CS*
F5RAM6_UDQS F5RAM6_D<15..0> F5RAM6_LDQS F5RAM6_UDM F5RAM6_LDM
F5RAM9_BA1 F5RAM9_BA0 F5RAM9_CK F5RAM9_CK* F5RAM9_CKE
F5RAM9_RAS* F5RAM9_CAS* F5RAM9_WE* F5RAM9_CS*
F5RAM9_UDQS F5RAM9_D<15..0> F5RAM9_LDQS F5RAM9_UDM F5RAM9_LDM
1V25 X 9

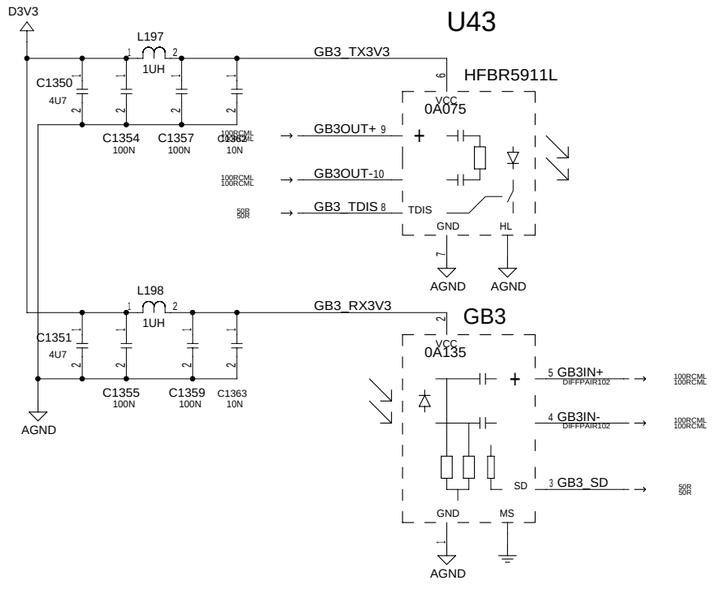
DEVELOPMENT

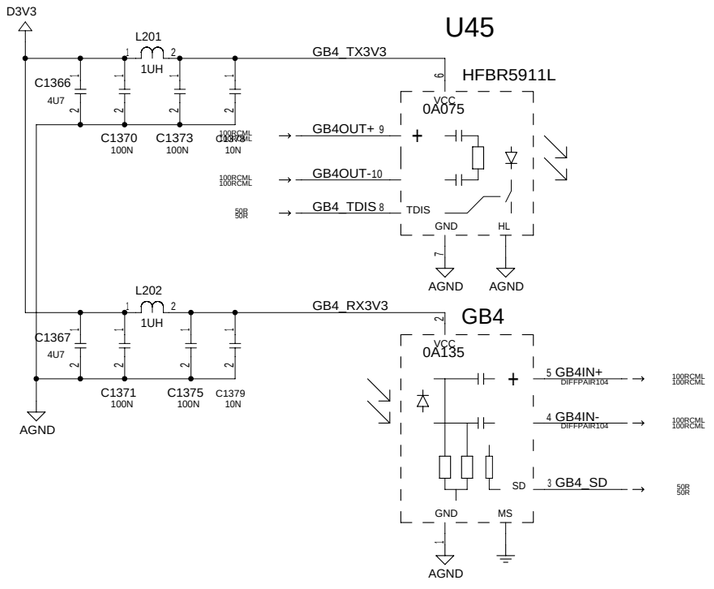
DRAWING

UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
FPGA5 RAMS 1 - 9		
Tue May 02 16:16:21 2006		
		SHEET 30 OF ??









DEVELOPMENT

DRAWING

UNIVERSITY OF CAMBRIDGE HEP

LHCB - RICHUKL1

4 X GB-TX/RX

Wed May 03 16:00:11 2006

SHEET 31 OF ??

U24

3V3

D3V3

C1381 L203 2U2 1A8 C65 C67 C69 C71
100U 6V3 4U7 100N 100N 10N

C1382 L204 2U2 1A8 C66 C68 C70 C72
100U 6V3 4U7 100N 100N 10N

AGND

4XGBE3V3IG

QTS

FPGA1 RS=33R AT FPGA1

R227 FPGA1_TX<31> 1 2 4XGBE_TX<31>
R228 FPGA1_TX<30> 2 4XGBE_TX<30>
R229 FPGA1_TX<29> 2 4XGBE_TX<29>
R230 FPGA1_TX<28> 2 4XGBE_TX<28>
R231 FPGA1_TX<27> 2 4XGBE_TX<27>
R232 FPGA1_TX<26> 2 4XGBE_TX<26>
R233 FPGA1_TX<25> 2 4XGBE_TX<25>
R234 FPGA1_TX<24> 2 4XGBE_TX<24>
R235 FPGA1_TX<23> 2 4XGBE_TX<23>
R236 FPGA1_TX<22> 2 4XGBE_TX<22>
R237 FPGA1_TX<21> 2 4XGBE_TX<21>
R238 FPGA1_TX<20> 2 4XGBE_TX<20>
R239 FPGA1_TX<19> 2 4XGBE_TX<19>
R240 FPGA1_TX<18> 2 4XGBE_TX<18>
R241 FPGA1_TX<17> 2 4XGBE_TX<17>
R242 FPGA1_TX<16> 2 4XGBE_TX<16>
R243 FPGA1_TX<15> 2 4XGBE_TX<15>
R244 FPGA1_TX<14> 2 4XGBE_TX<14>
R245 FPGA1_TX<13> 2 4XGBE_TX<13>
R246 FPGA1_TX<12> 2 4XGBE_TX<12>
R247 FPGA1_TX<11> 2 4XGBE_TX<11>
R948 FPGA1_TX<10> 2 4XGBE_TX<10>
R958 FPGA1_TX<9> 2 4XGBE_TX<9>
R968 FPGA1_TX<8> 2 4XGBE_TX<8>
R1017 FPGA1_TX<7> 2 4XGBE_TX<7>
R1018 FPGA1_TX<6> 2 4XGBE_TX<6>
R1019 FPGA1_TX<5> 2 4XGBE_TX<5>
R1020 FPGA1_TX<4> 2 4XGBE_TX<4>
R1021 FPGA1_TX<3> 2 4XGBE_TX<3>
R1022 FPGA1_TX<2> 2 4XGBE_TX<2>
R1023 FPGA1_TX<1> 2 4XGBE_TX<1>
R1024 FPGA1_TX<0> 2 4XGBE_TX<0>

→ 4XGBE_TX<31..0>

TX 3V3 - LVTTL

4 TDAT31
1 TDAT30
5 TDAT29
2 TDAT28
3 TDAT27
9 TDAT26
6 TDAT25
7 TDAT24
13 TDAT23
11 TDAT22
8 TDAT21
15 TDAT20
10 TDAT19
17 TDAT18
19 TDAT17
12 TDAT16
21 TDAT15
23 TDAT14
14 TDAT13
25 TDAT12
16 TDAT11
27 TDAT10
29 TDAT9
18 TDAT8
31 TDAT7
33 TDAT6
20 TDAT5
35 TDAT4
37 TDAT3
22 TDAT2
24 TDAT1
39 TDAT0

3V3 - 10W MAX VCC

RX 3V3 - LVTTL RS=33R

RDAT31 63
RDAT30 59
RDAT29 65
RDAT28 62
RDAT27 67
RDAT26 71
RDAT25 69
RDAT24 64
RDAT23 68
RDAT22 73
RDAT21 66
RDAT20 70
RDAT19 72
RDAT18 75
RDAT17 74
RDAT16 77
RDAT15 79
RDAT14 76
RDAT13 81
RDAT12 78
RDAT11 83
RDAT10 80
RDAT9 85
RDAT8 82
RDAT7 87
RDAT6 88
RDAT5 84
RDAT4 86
RDAT3 89
RDAT2 90
RDAT1 91
RDAT0 93

→ 4XGBE_RX<31..0> → FPGA1

FPGA1 RS=33R AT FPGA1

R1025 FPGA1_TFCLK 4XGBE_TFCLK 41 TFCLK
R1026 FPGA1_TSXK 4XGBE_TSXK 43 TSX
R1027 FPGA1_TSOP 4XGBE_TSOP 45 TSOP
R1028 FPGA1_TPRTY 4XGBE_TPRTY 47 TPRTY
R1029 FPGA1_TENB 4XGBE_TENB 26 TENB
R1030 FPGA1_TEOP 4XGBE_TEOP 28 TEOP
R1031 FPGA1_TMOD1 4XGBE_TMOD1 30 TMOD1
R1032 FPGA1_TMOD0 4XGBE_TMOD0 32 TMOD0
R1033 FPGA1_TERR 4XGBE_TERR 34 TERR
R1034 FPGA1_TADR0 4XGBE_TADR0 36 TADR0
R1035 FPGA1_TADR1 4XGBE_TADR1 42 TADR1
4XGBE_STPA 38 STPA 33R
4XGBE_PTPA 40 PTPA

RSOP 53 4XGBE_RSOP → FPGA1
RMOD0 55 4XGBE_RMOD0 → FPGA1
RMOD1 57 4XGBE_RMOD1 → FPGA1
RVAL 52 4XGBE_RVAL → FPGA1
REOP 54 4XGBE_REOP → FPGA1
RSX 56 4XGBE_RSX → FPGA1
RERR 58 4XGBE_RERR → FPGA1
RPRTY 60 4XGBE_RPRTY → FPGA1
RENB 51 4XGBE_RENB ← FPGA1
RFCLK 61 4XGBE_RFCLK ← FPGA1

4XGBE_RENB R1038 FPGA1_RENB
4XGBE_RFCLK R1039 FPGA1_RFCLK
RS=33R AT FPGA1

4XGBE_TXPAUSEFR 49 TXPAUSEFR HARDMOD
4XGBE_TXPAUSEADD0 46 TXPAUSEADD0
4XGBE_TXPAUSEADD1 48 TXPAUSEADD1 2V5
4XGBE_TXPAUSEADD2 50 TXPAUSEADD2

GBE_TXPAUSEFR → R256 2
GBE_TXPAUSEADD0 → R257 2
GBE_TXPAUSEADD1 → R258 2
GBE_TXPAUSEADD2 → R259 2

U23 74LVC244A
2V5E1
C63 100N
VCC 20
1A1 2 1Y1 18
1A2 4 1Y2 16
1A3 6 1Y3 14
1A4 8 1Y4 12
1OE* 1
2A1 11 2Y1 9
2A2 13 2Y2 7
2A3 15 2Y3 5
2A4 17 2Y4 3
2OE* 19
GND 10
DGND

TTCTDO_GBETDI → R260 2
JTAG_RST* → R261 2
GBE_TCK → R262 2
GBE_TMS → R263 2

GLUECARD → 4XGBE_LA<13..2>
RS=33R AT GLUECARD (EXT)

CONTROL 3V3 - LVTTL

145 BAD1
120 AD10
135 AD9
133 AD8
118 AD7
131 AD6
129 AD5
116 AD4
127 AD3
125 AD2
123 AD1
114 AD0

GLUECARD → 4XGBE_WR* 122 WR*
GLUECARD → 4XGBE_RD* 137 RD*
GLUECARD → 4XGBE_CS* 139 CS*
GLUECARD ← PLX_READY* 141 RDY*
BAD0 143

PLX_READY* R267 22R C1380 22P AGND
R268 33R 3V3

3V3 - LVTTL

D15 121
D14 112
D13 119
D12 110
D11 117
D10 115
D9 108
D8 113
D7 111
D6 106
D5 109
D4 107
D3 104
D2 105
D1 103
D0 102

4XGBE_D<15..0> ↔ GLUECARD

4XGBE_D<15> R269 C1383 22P
4XGBE_D<14> R270 C1384 22P
4XGBE_D<13> R271 C1385 22P
4XGBE_D<12> R272 C1386 22P
4XGBE_D<11> R273 C1387 22P
4XGBE_D<10> R274 C1388 22P
4XGBE_D<9> R275 C1389 22P
4XGBE_D<8> R276 C1390 22P
4XGBE_D<7> R277 C1391 22P
4XGBE_D<6> R278 C1392 22P
4XGBE_D<5> R279 C1393 22P
4XGBE_D<4> R280 C1394 22P
4XGBE_D<3> R281 C1395 22P
4XGBE_D<2> R282 C1396 22P
4XGBE_D<1> R283 C1397 22P
4XGBE_D<0> R284 C1398 22P
MOUNT CLOSE TO QTS CONNECTOR
AGND

R264 0R R266 0R

4XGBE_TDI 124 TDI
4XGBE_TDO 126 TDO
4XGBE_TRST* 128 TRSTB*
4XGBE_TCLK 130 TCLK
4XGBE_TMS 132 TMS
(2V5)
JTAG

C64 100N 2V5E1 U48 G125
GBE_TDO ← 6 1Y 1A 2
OE* 1
3 2Y 2A 5
OE* 7
GND 4
DGND

2V5 3V3

EEPROM (3V3)
SCL 146 SCL ↔ TTC
SDA 147 SDA ↔ TTC
EA0 148
EA1 142
EA2 144
WP 147 4XGBE_WP ← FPGA1

GLUECARD → 4XGBE_CI816 92 CI816 (3V3) (2V5)
200MS → MRESET* 101 SYSRES (3V3)
0R

CONF1 134 4XGBE_CONF1 → FPGA1
CONF0 136 4XGBE_CONF0 → FPGA1

POL GND DNC 0R

U1U24_1 U24.100
U1U24_2 U24.98
U1U24_3 U24.96
U1U24_4 U24.97
U1U24_5 U24.99
U1U24_6 U24.95

AGND

EXTRA CONNECTIONS

NORMAL OPERATION = FIT R265/R266 - NO FIT R264
BYPASS = FIT R264 - NO FIT R265/R266

DEVELOPMENT

DRAWING

UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
QUAD GIGABIT ETHERNET (4XGBE)		
Wed Jun 07 15:26:41 2006		
		SHEET 32 OF ??

INDUCTOR ?

D5V

C1399 470U 10V

C1400 C1401 C1402 C1403 C1404 C1405 C1406 C1407 C1408 C1409 C1410 C1411 C1412 C1413 C1414

4U7 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N 100N

DGND

RS232 (5V TTL/CMOS)

GC J3

B1	J3B1	DCD1	J3A1	A1
B2	J3B2	DSR1	J3A2	A2
B3	J3B3	RXD1	J3A3	A3
B4	J3B4	RTS1	J3A4	A4
B5	J3B5	TXD1	J3A5	A5
B6	J3B6	CTS1	J3A6	A6
B7	J3B7	DTR1	J3A7	A7
B8	J3B8	RI1	J3A8	A8
B9	J3B9	DCD2	J3A9	A9
B10	J3B10	DSR2	J3A10	A10
B11	J3B11	RXD2	J3A11	A11
B12	J3B12	RTS2	J3A12	A12
B13	J3B13	TXD2	J3A13	A13
B14	J3B14	CTS2	J3A14	A14
B15	J3B15	DTR2	J3A15	A15
B16	J3B16	RI2	J3A16	A16
B17	J3B17	INDEX	J3A17	A17
B18	J3B18	DRVSEL1	J3A18	A18
B19	J3B19	DSKCHG	J3A19	A19
B20	J3B20	MTR1	J3A20	A20
B21	J3B21	DIR	J3A21	A21
B22	J3B22	STEP	J3A22	
B23	J3B23	WRDATA	J3A23	A23
B24	J3B24	WRGATE	J3A24	A24
B25	J3B25	TRK0	J3A25	A25
B26	J3B26	WRPT	J3A26	A26
B27	J3B27	RDATA	J3A27	A27
B28	J3B28	HDSEL	J3A28	A28
B29	J3B29	DRVSEL0	J3A29	A29
B30	J3B30	MTR0	J3A30	A30
B31	J3B31	NC	J3A31	A31
B32	J3B32	IDIRST*	J3A32	A32
B33	J3B33	NC	J3A33	A33
B34	J3B34	USBP0+	J3A34	A34
B35	J3B35	USBP0-	J3A35	A35
B36	J3B36	A0	J3A36	A36
B37	J3B37	A1	J3A37	A37
B38	J3B38	A2	J3A38	A38
B39	J3B39	IORDY	J3A39	A39
B40	J3B40	D3232	J3A40	A40
B41	J3B41	IRDATX	J3A41	A41
B42	J3B42	IRDARX	J3A42	A42
B43	J3B43	D33	J3A43	A43
B44	J3B44	D34	J3A44	A44
B45	J3B45	D35	J3A45	A45
	J3B46	3VBAT	J3A46	
B47	J3B47	AD16	J3A47	A47
B48	J3B48	AD17	J3A48	A48
B49	J3B49	AD18	J3A49	A49
B50	J3B50	AD19	J3A50	A50
B51	J3B51	AD20	J3A51	A51
B52	J3B52	AD21	J3A52	A52
B53	J3B53	AD22	J3A53	A53
B54	J3B54	AD23	J3A54	A54
B55	J3B55	AD24	J3A55	A55
B56	J3B56	AD25	J3A56	A56
B57	J3B57	AD26	J3A57	A57
B58	J3B58	AD27	J3A58	A58
B59	J3B59	AD28	J3A59	A59
B60	J3B60	AD29	J3A60	A60
B61	J3B61	AD30	J3A61	A61
B62	J3B62	AD31	J3A62	A62
B63	J3B63	PIRQA	J3A63	A63
B64	J3B64	PIRQB	J3A64	A64
B65	J3B65	PIRQC	J3A65	A65
B66	J3B66	PIRQD	J3A66	A66
	J3B67	5V	J3A67	
B68	J3B68	CLK2	J3A68	A68
B69	J3B69	GNT0*	J3A69	A69
B70	J3B70	GNT1*	J3A70	A70
B71	J3B71	GNT2*	J3A71	A71
B72	J3B72	GNT3*	J3A72	A72
	J3B73	5V	J3A73	
B74	J3B74	IRDY*	J3A74	A74
B75	J3B75	STOP*	J3A75	A75
B76	J3B76	PAR*	J3A76	A76
B77	J3B77	LOCK*	J3A77	A77
B78	J3B78	PCIRST*	J3A78	
B79	J3B79	NC	J3A79	
B80	J3B80	DACK7	J3A80	A80
B81	J3B81	USBP1+	J3A81	A81
B82	J3B82	USBP1-	J3A82	A82
B83	J3B83	NC	J3A83	A83
B84	J3B84	NC	J3A84	A84
B85	J3B85	LA22	J3A85	A85
B86	J3B86	LA23	J3A86	A86
B87	J3B87	PERR-	J3A87	A87
B88	J3B88	NC	J3A88	A88
B89	J3B89	SMBDAT	J3A89	A89
B90	J3B90	SMBCLK	J3A90	A90
	J3B91	CC3V3	J3A91	
B92	J3B92	NC	J3A92	
B93	J3B93	IOCHK	J3A93	
B94	J3B94	TCK	J3A94	
B95	J3B95	TDI	J3A95	
B96	J3B96	TDO	J3A96	
B97	J3B97	TMS	J3A97	A97
B98	J3B98	DDA	J3A98	A98
B99	J3B99	DDC	J3A99	A99
B100	J3B100	GPIO7	J3A100	A100
B101	J3B101	ANGND	J3A101	A101
B102	J3B102	VSYNC	J3A102	A102
B103	J3B103	HSYNC	J3A103	A103
B104	J3B104	ENAVDD	J3A104	A104
B105	J3B105	SHCLK	J3A105	
B106	J3B106	LPHS	J3A106	A106
B107	J3B107	D0	J3A107	A107
B108	J3B108	D1	J3A108	A108
B109	J3B109	D2	J3A109	A109
B110	J3B110	D3	J3A110	A110
B111	J3B111	D4	J3A111	A111
B112	J3B112	D5	J3A112	A112
B113	J3B113	D6	J3A113	A113
B114	J3B114	D7	J3A114	A114
B115	J3B115	D8	J3A115	A115
B116	J3B116	D9	J3A116	A116
B117	J3B117	D10	J3A117	A117
B118	J3B118	D11	J3A118	A118
B119	J3B119	LCDM	J3A119	A119
	J3B120	COREV	J3A120	

3V3 STR* AUTO* ERROR* INIT* SLCTIN* PRND0 PRND1 PRND2 PRND3 PRND4 PRND5 PRND6 PRND7 ACK* BUSY PAPEND SEL KBDAT KBCLK MCLK MDAT GND HD D0 HD D1 HD D2 HD D3 HD D4 HD D5 HD D6 HD D7 HD D8 HD D9 HD D10 HD D11 HD D12 HD D13 HD D14 HD D15 CS0* CS1* PDACK* PREQ IRQ IOR* IOW* 5V AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 BE0* BE1* BE2* BE3* 5V CLK1 REQ0* REQ1* REQ2* REQ3* ACLED FRAME* TRDY* DEVSEL* SERR* LILED CCRST NC D24 D25 D26 D27 D28 D29 D30 D31 ROMRD ROMWR CC3V3 LAN TX+ LAN TX- LAN RX+ LAN RX- NC VCCSUS SUSA SUSB GPIO2 GRN BLU RED ENAVEE GND FLMVS D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 ENBK LCDV

PAD 0.9 0.7 PAD

J3G1 J3P2 J3P1 J3G2

DGND

GC

GC J4

4XGBE ← 4XGBE_LA<13..2>

J4A60 J4B60 J4B59 J4A57 J4A56 J4A54 J4A115 J4A111 J4A110 J4A109 J4A98 J4A47 J4A46 J4A97 J4A96 J4A43 J4A42 J4A36 J4A95 J4A89 J4A88 J4A87

LA23 LA22 LA21 LA20 LA19 LA18 LA17 LA16 LA15 LA14 LA13 LA12 LA11 LA10 LA9 LA8 LA7 LA6 LA5 LA4 LA3 LA2

PLX

GC_ADS* GC_BLAST* GC_CS1* GC_LW/R* PLX_READY*

C1417 C1415 C1418 C1416 C1419 R287 R285 R288 R286 R289

AGND

FPGA1 ← GC_ADS* J4A21 ADS*
FPGA1 ← GC_BLAST* J4A31 BLAST*
FPGA1 ← GC_CS1* J4A27 CS1*
FPGA1 ← GC_LW/R* J4A22 LW/R*
FPGA1 → PLX_READY* J4A25 READY*
J4A26 CS0*
J4A30 LRESET
FPGA1 → 20MHZ J4A23 ALE
J4A32 LCLK
FPGA1 → GC_LINT1 J4A33 LINT2
J4A40 LINT1
J4A39 LBE3*
J4A38 LBE2*
J4A37 LBE1*
J4A44 LBE0*
J4A45 LREQ
J4A58 LGNT
4XGBE ← 4XGBE_RD* J4A59 RD*
4XGBE ← 4XGBE_WR* WR*
J4A108 BTERM*
J4A116 BCLK

3V3

PROMS VIA BUFFER FPGA1 ← GC_CONFIG* ECS_RESET*

J4A53 GPIO8
J4A52 GPIO7
J4A51 GPIO6
J4A50 GPIO5
J4A49 GPIO4
J4A107 GPIO3
4XGBE ← 4XGBE_CS* J4A106 GPIO2
J4A105 GPIO1
J4A94 GPIO0

MRESET* → J4B98 → RESET*
200MS

PAD 0.9 0.7 PAD

J4G1 J4P2 J4P1 J4G2

DGND

GND RSV NC

U25

C1421 C1422 C1423 C1424 C1425 C1426 C1427 C1428 C1429 C1430 C1431

100N 100N 100N 100N 100N 100N 100N 100N 100N 4U7 100U 6V3

D3V3

DGND

5V 0A04 3V3 0A3

PLX

LAD31 LAD30 LAD29 LAD28 LAD27 LAD26 LAD25 LAD24 LAD23 LAD22 LAD21 LAD20 LAD19 LAD18 LAD17 LAD16 LAD15 LAD14 LAD13 LAD12 LAD11 LAD10 LAD9 LAD8 LAD7 LAD6 LAD5 LAD4 LAD3 LAD2 LAD1 LAD0

J4B18 J4B17 J4B16 J4B15 J4B14 J4B13 J4B12 J4B11 J4B9 J4B8 J4B7 J4B6 J4B5 J4B4 J4B3 J4B2 J4A19 J4A18 J4A17 J4A16 J4A15 J4A14 J4A13 J4A12 J4A10 J4A9 J4A8 J4A7 J4A6 J4A5 J4A4 J4A3

↔ FPGA1

4XGBE_D<15..0>

↔ 4XGBE

4XGBE_D<15> R328 4XGBE_D<14> R344 4XGBE_D<13> R329 4XGBE_D<12> R345 4XGBE_D<11> R330 4XGBE_D<10> R346 4XGBE_D<9> R331 4XGBE_D<8> R347 4XGBE_D<7> R332 4XGBE_D<6> R348 4XGBE_D<5> R333 4XGBE_D<4> R349 4XGBE_D<3> R334 4XGBE_D<2> R350 4XGBE_D<1> R335 4XGBE_D<0> R351

51R 22P C1440 C1441 C1442 C1443 C1444 C1445 C1446 C1447

AGND

MOUNT CLOSE TO GLUECARD CONNECTOR J4

JTAG

JPWR3 J4A119
TCK3 J4B115 GC_TCK3 → ALL DEVICES
TDO3 J4B116 GC_TDO3 ← ALL DEVICES
TMS3 J4B117 GC_TMS3 → ALL DEVICES
TDI3 J4B118 GC_TDI3 → ALL DEVICES
TRES3 J4B119 GC_RST3* → TTCRX

JPWR2 J4A118
TCK2 J4B32 CONFPGA_TCK →
TDO2 J4B33 CONFPGA_TDO ←
TMS2 J4B34 CONFPGA_TMS →
TDI2 J4B35 CONFPGA_TDI →
TRES2 J4B36

JPWR1 J4A117
TCK1 J4B26 CONPROM_TCK →
TDO1 J4B27 CONPROM_TDO ←
TMS1 J4B28 CONPROM_TMS →
TDI1 J4B29 CONPROM_TDI →
TRES1 J4B30

D3V3

1K0 R304 R306 R308 R3102 R3112 R3114 R3116 R3118

I2C

SDA4 SCL4 J4B55 J4B56
SDA3 SCL3 J4B52 J4B53
SDA2 SCL2 J4B49 J4B50 GC_SDA GC_SCL ↔ ALLDEVICES
SDA1 SCL1 J4B46 J4B47

PL3

RS232

DCDV1 J4B61 DCDV1 1
RXDV1 J4B62 RXDV1 2
TXDV1 J4B63 TXDV1 3
DTRV1 J4B64 DTRV1 4
5
DSRV1 J4B66 DSRV1 6
RTSV1 J4B67 RTSV1 7
CTSV1 J4B68 CTSV1 8
RTV1 J4B69 RTV1 9

RS232 (+/- 10V)

DTYPE9

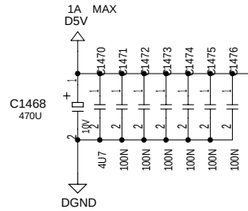
4K7 R305 R307 R309 R3113 R3115 R3117 R3119

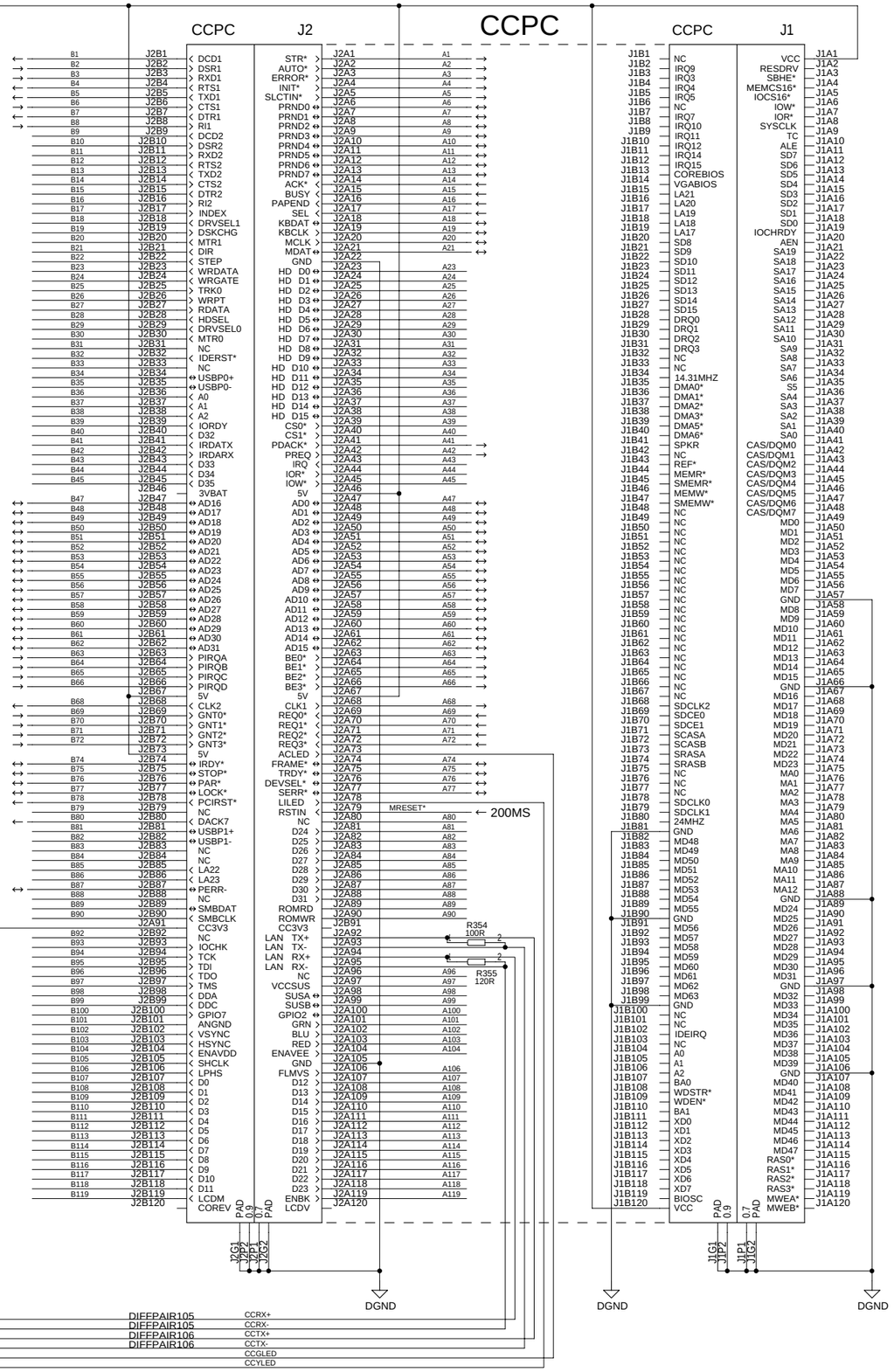
DEVELOPMENT

DRAWING

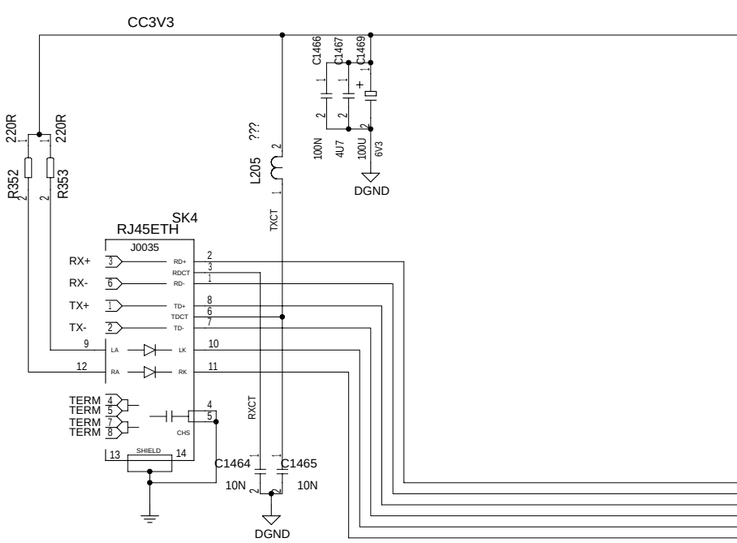
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
GLUECARD		
Tue Jun 13 12:07:41 2006		
		SHEET 33 OF ??

CCPC1





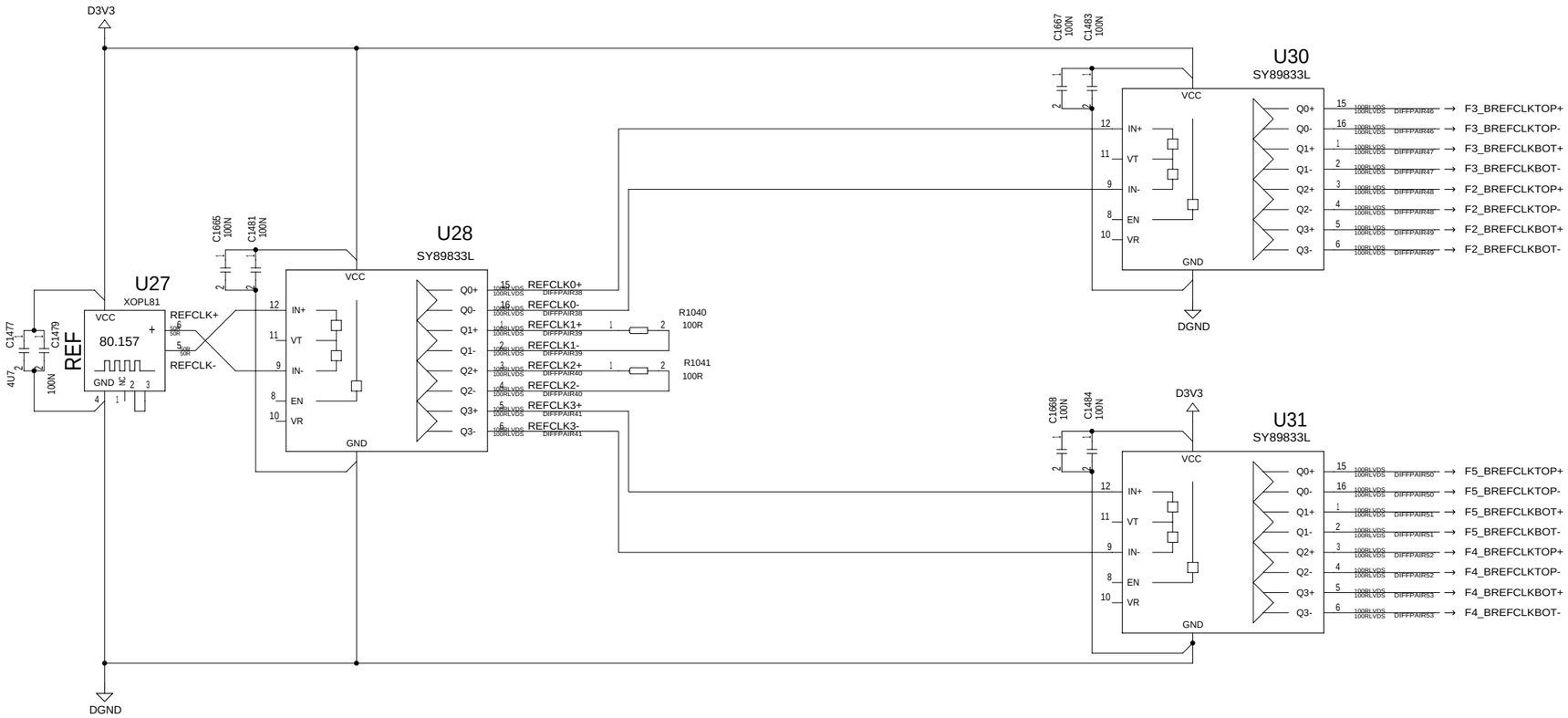
QUERY TDCT PULL-UP ?



DEVELOPMENT

DRAWING

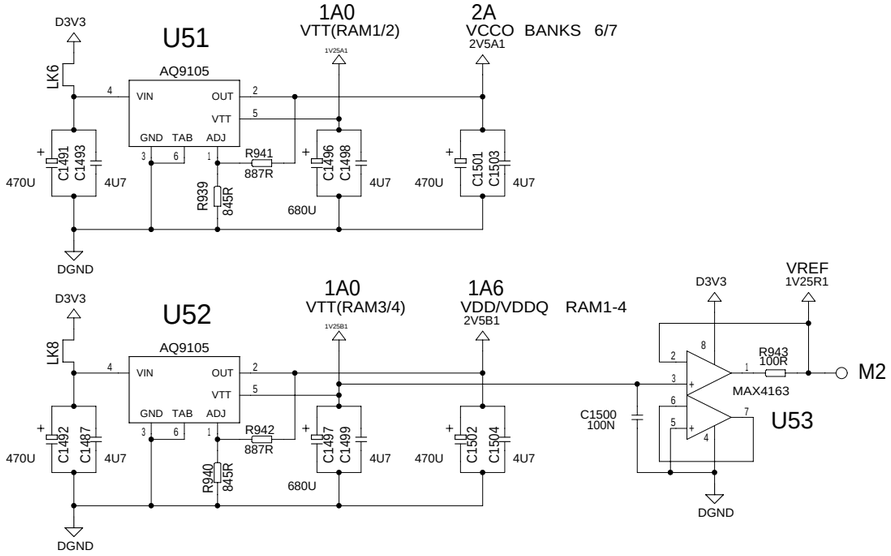
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
CREDIT CARD PC		
Tue Jun 13 09:44:57 2006		
		SHEET 34 OF ??

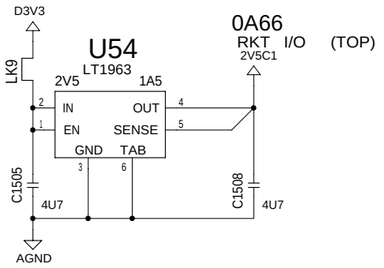


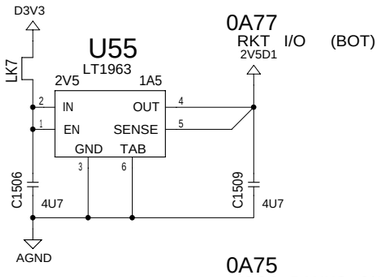
DEVELOPMENT

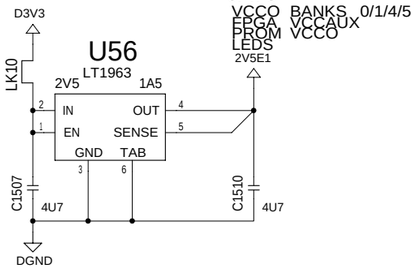
DRAWING

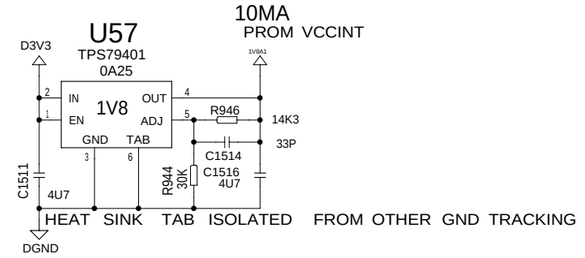
UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
CLOCKS		
Wed May 03 16:03:32 2006		
		SHEET 35 OF ??

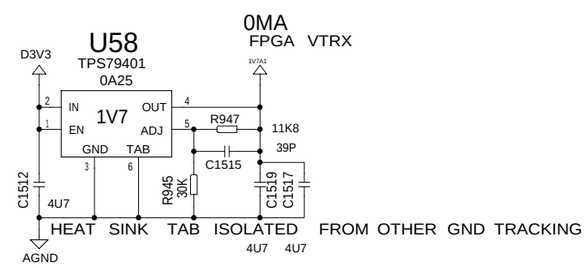


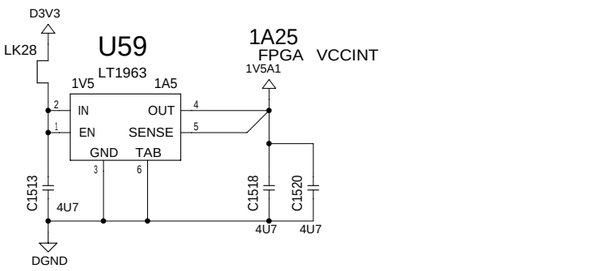




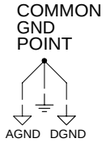


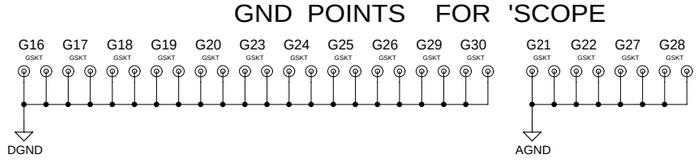






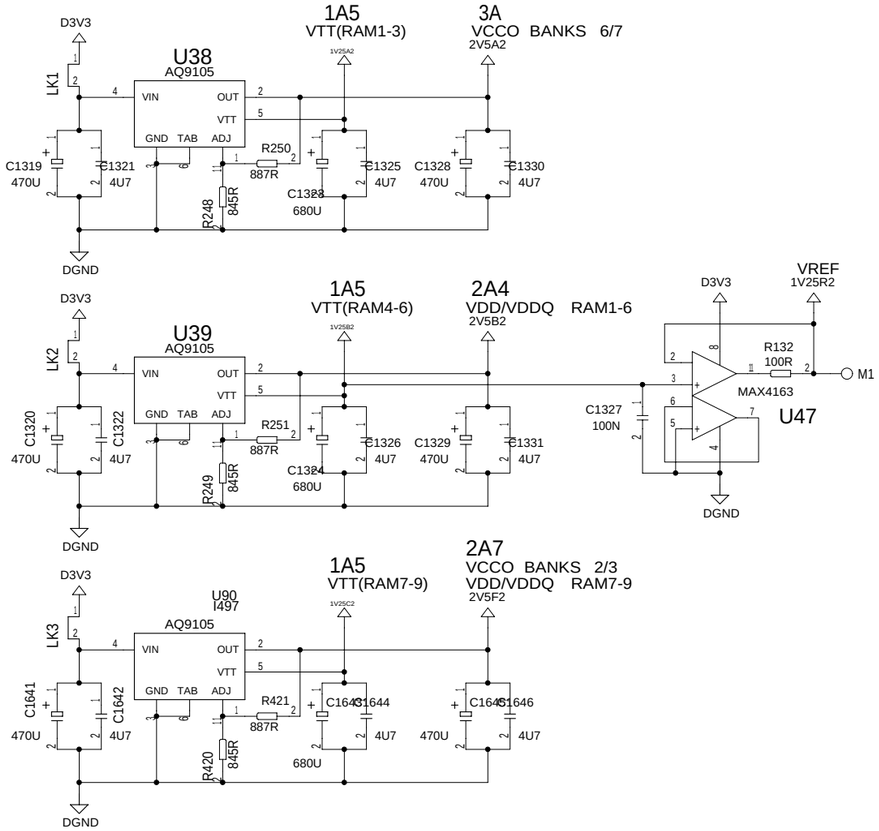
PWR1	=	1V7/2V5A/2V5C/2V5D
PWR2	=	2V5B/2V5E/3V3/VCCRX/VCCTX/ETHVCCD
PWR3	=	1V25A/1V25B/1V5/1V7
PWR4	=	3V3 NOT SURE YET
GND1	=	ANA
GND2	=	ANA
GND3	=	DIG
GND4	=	DIG





DRAWING DEVELOPMENT

UNIVERSITY OF CAMBRIDGE HEP		
LHCB - RICHUKL1		
VOLTAGE REGULATORS - AREA 1		
Thu Jun 08 10:31:56 2006		
		SHEET 36 OF 41



PWR1 = 1V7/2V5A/2V5C/2V5D

PWR2 = 2V5B/2V5E/3V3/VCCRX/VCCTX/ETHVCCD

PWR3 = 1V25A/1V25B/1V25C/1V5/1V7

PWR4 = 3V3

GND1 = ANA

GND2 = ANA

GND3 = DIG

GND4 = DIG

DEVELOPMENT

DRAWING

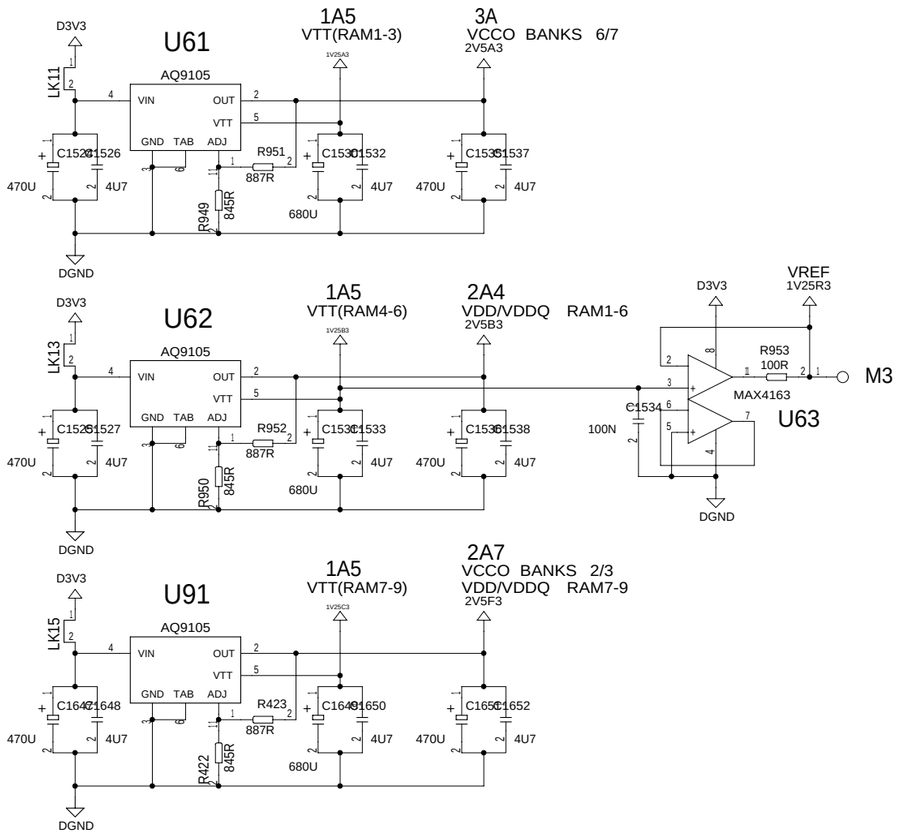
UNIVERSITY OF CAMBRIDGE HEP

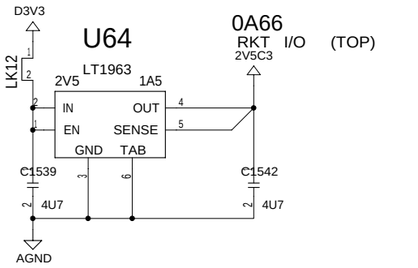
LHCB - RICHUKL1

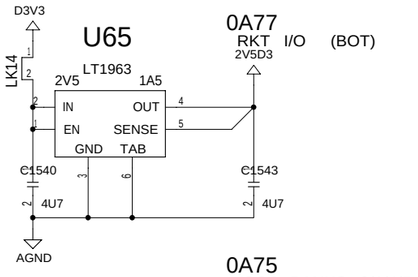
VOLTAGE REGULATORS - AREA 2

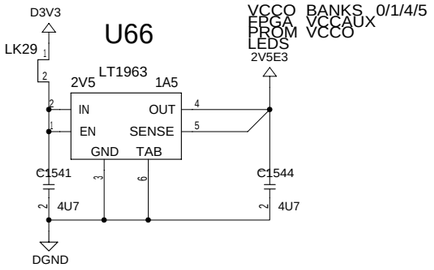
Wed May 03 16:10:09 2006

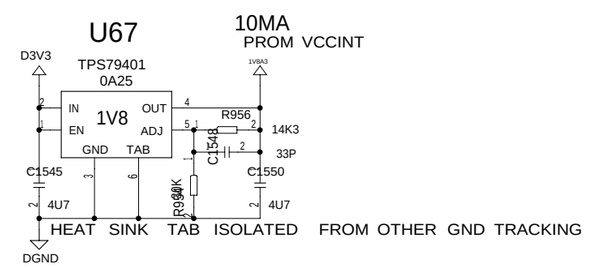
SHEET 37 OF ??

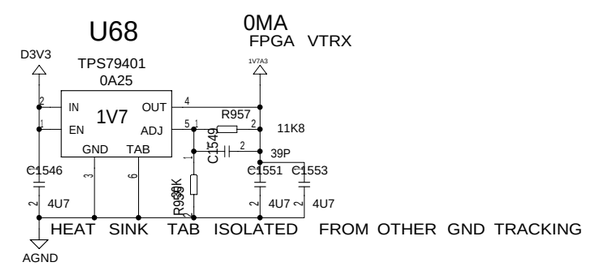


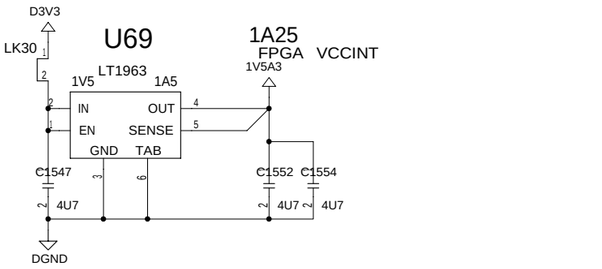












PWR1 = 1V7/2V5A/2V5C/2V5D

PWR2 = 2V5B/2V5E/3V3/VCCRX/VCCTX/ETHVCCD

PWR3 = 1V25A/1V25B/1V25C/1V5/1V7

PWR4 = 3V3

GND1 = ANA

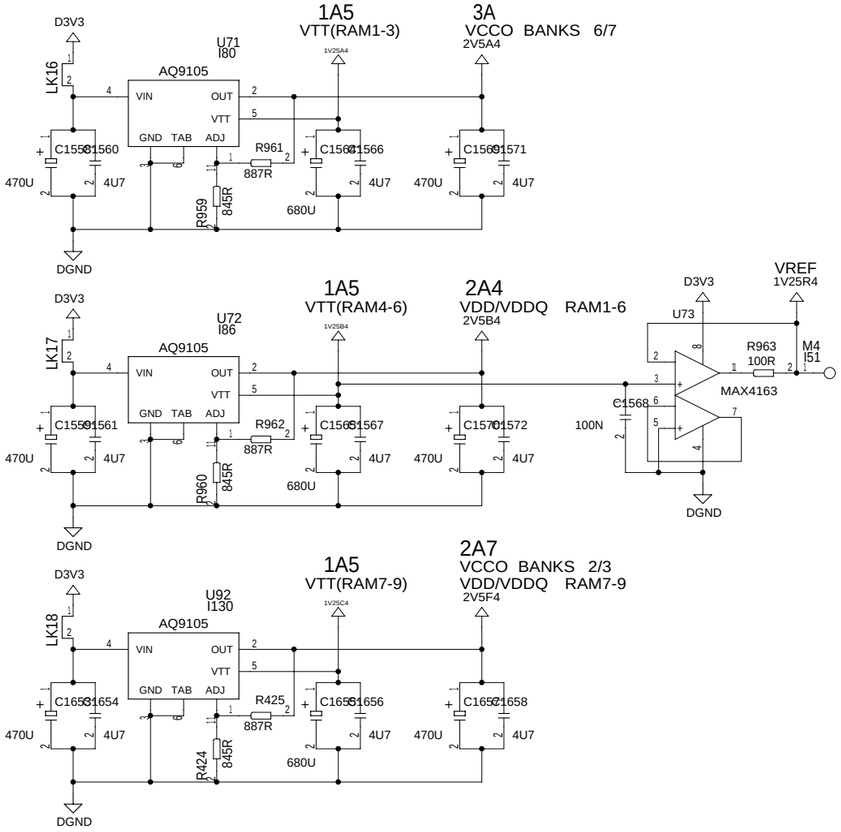
GND2 = ANA

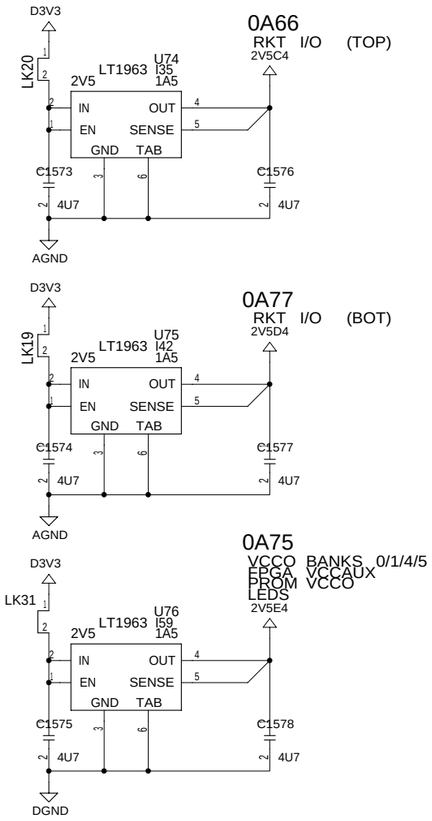
GND3 = DIG

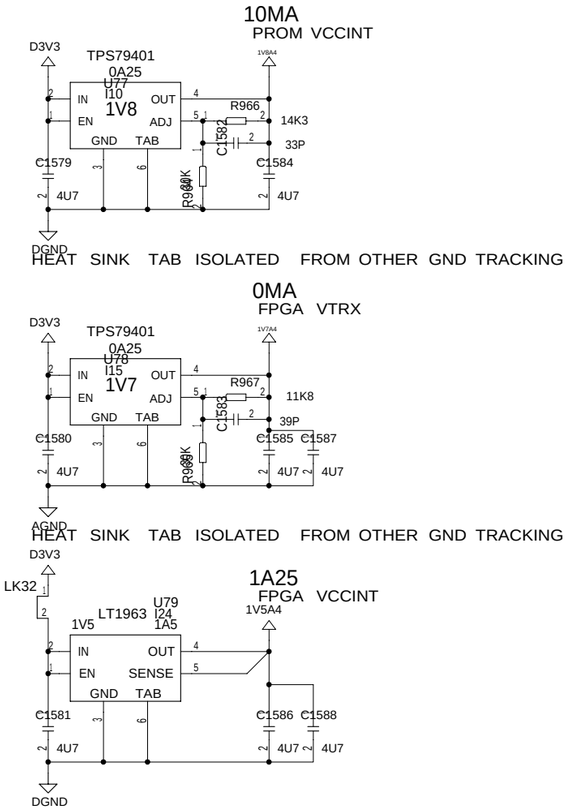
GND4 = DIG

DRAWING **DEVELOPMENT**

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LHCB - RICHUKL1		
VOLTAGE REGULATORS - AREA 3		
Wed May 03 16:12:49 2006		
		SHEET 38 OF ??







PWR1 = 1V7/2V5A/2V5C/2V5D

PWR2 = 2V5B/2V5E/3V3/VCCRX/VCCTX/ETHVCCD

PWR3 = 1V25A/1V25B/1V25C/1V5/1V7

PWR4 = 3V3

GND1 = ANA

GND2 = ANA

GND3 = DIG

GND4 = DIG

DEVELOPMENT

DRAWING

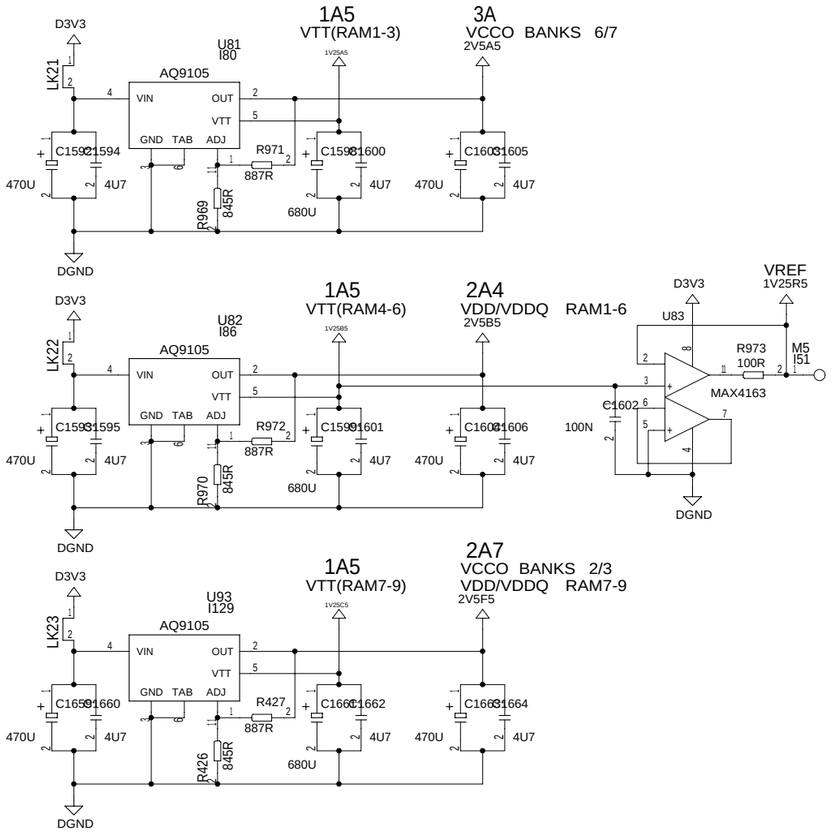
UNIVERSITY OF CAMBRIDGE HEP

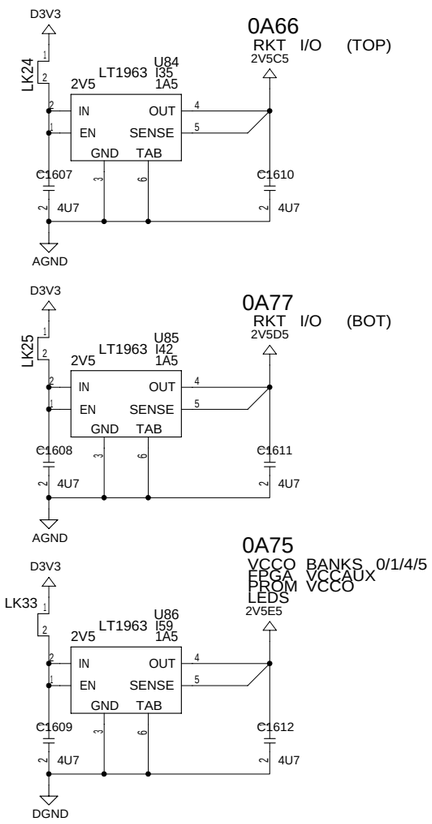
LHCB - RICHUKL1

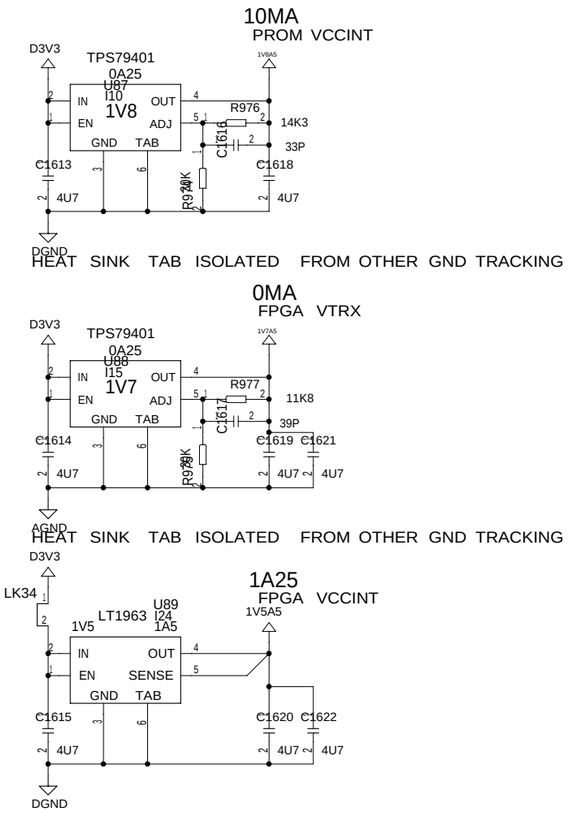
VOLTAGE REGULATORS - AREA 4

Wed May 03 16:15:36 2006

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PWR1 = 1V7/2V5A/2V5C/2V5D

PWR2 = 2V5B/2V5E/3V3/VCCRX/VCCTX/ETHVCCD

PWR3 = 1V25A/1V25B/1V25C/1V5/1V7

PWR4 = 3V3

GND1 = ANA

GND2 = ANA

GND3 = DIG

GND4 = DIG

DEVELOPMENT

DRAWING

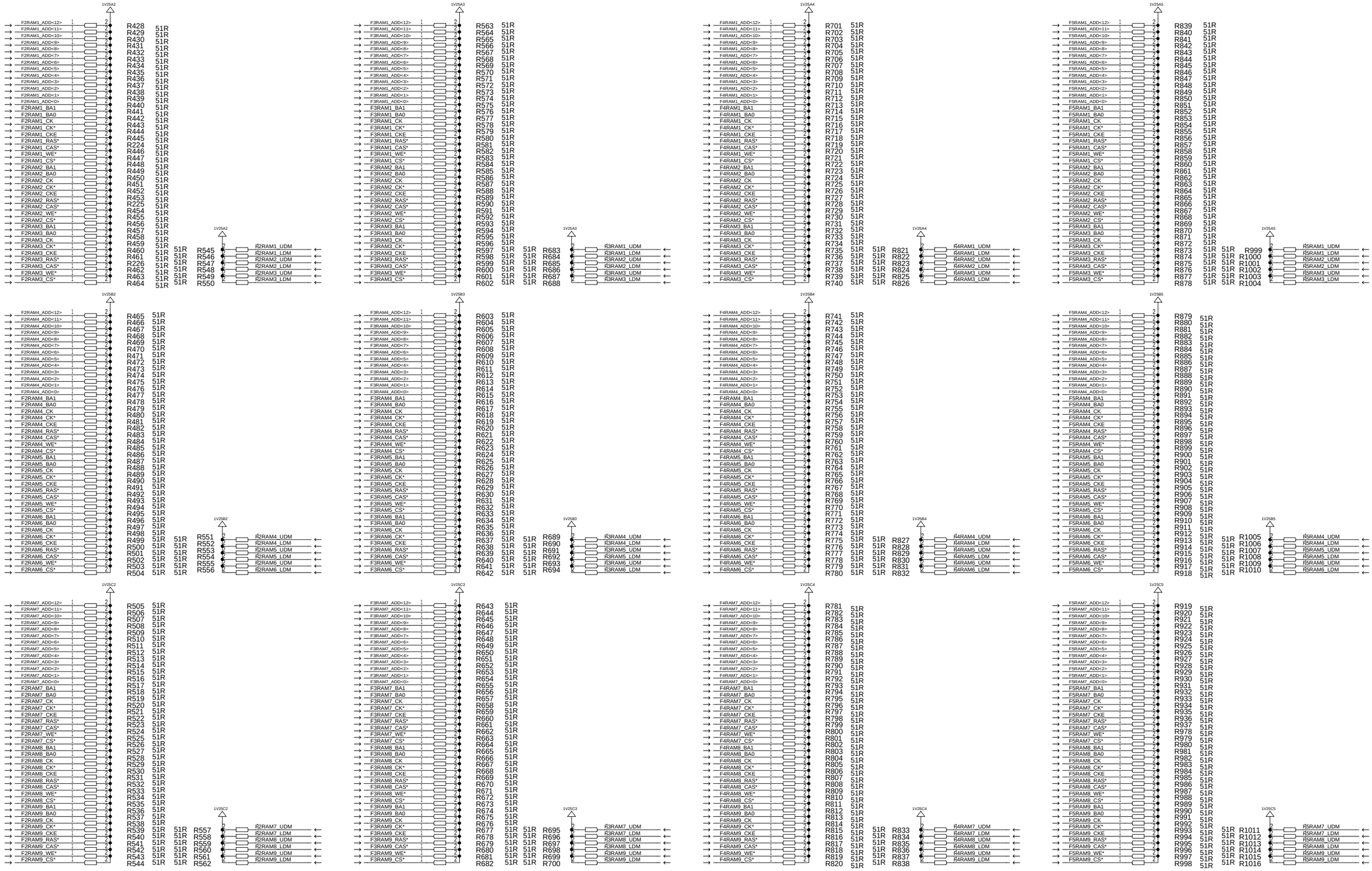
UNIVERSITY OF CAMBRIDGE HEP

LHCB - RICHUKL1

VOLTAGE REGULATORS - AREA 5

Wed May 03 16:18:23 2006

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DEVELOPMENT

DRAWING

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LHCB - RICHUKL1

F2-F5 RAM TERMINATIONS

Tue May 02 16:16:45 2006

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