Ophio

Features

Ophio is a 4-channel Gigabit optical receiver which couples to the Chimaera module. The optical receiver module is a 12-channel Agilent or Emcore part of which channels 8 to 11 are decoded using Texas deserialisers. The module requires a 5V power supply which is usually provided through the Chimaera coupling connector but can also be provided by a bench top supply for standalone tests.

Connectors and indicators

Status LEDs

A bank of eight LEDs are provided at the front panel. These are connected to pins of the Chimaera FPGA through the coupling connector to provide programmable functionality.

Two pole LEMO00 front panel connector

This connector is coupled to a pair of Chimaera FPGA IO pins via the coupling connector. The pins may be programmed by the application as either single ended or differential IO. The Chimaera board has provision for mounting terminating resistors when the connector is configured as an input.

Front-end coupling connector, SKT1

Ophio is normally connected to the Chimaera. This connector provides power to Ophio and links Chimaera FPGA IO pins to the Ophio signals.

Pin	Ophio function	FPGA pin	Pin	Ophio function	FPGA pin	Pin	Ophio function	FPGA pin
1A	LED1A	U9	1B	LED1B	U10	1C	LED2A	V10
2A	LED2B	V11	2B	LED3A	W6	2C	LED3B	V9
3A	LED4A	AB11	3B	LED4B	AA6	3C	N/A	NC
4A	RXD_A(15)	AB10	4B	RXERR_A	W11	4C	RXD_A(14)	Y11
5A	RXD_A(13)	AA10	5B	RXDVLOS_A	W10	5C	RXD_A(12)	Y10
6A	RXD_A(11)	AB9	6B	GND	NC	6C	RXD_A(10)	Y9
7A	GND	NC	7B	RXCLK_A	W9	7C	GND	NC
8A	RXD_A(9)	AA9	8B	N/A	V8	8C	RXD_A(8)	W9
9A	RXD_A(7)	AB8	9B	N/A	V7	9C	RXD_A(6)	W7
10A	RXD_A(5)	AA8	10B	N/A	AB5	10C	RXD_A(4)	AB6
11A	RXD_A(3)	AB7	11B	N/A	W5	11C	RXD_A(2)	Y5
12A	RXD_A(1)	AA7	12B	N/A	AA3	12C	RXD_A(0)	AB3
13A	VCC	NC	13B	VCC	NC	13C	VCC	NC
14A	VCC	NC	14B	VCC	NC	14C	VCC	NC
15A	VCC	NC	15B	VCC	NC	15C	VCC	NC
16A	RXD_B(15)	U2	16B	RXERR_B	W3	16C	RXD_B(14)	Y2
17A	RXD_B(13)	U1	17B	RXDVLOS_B	V2	17C	RXD_B(12)	W1
18A	RXD_B(11)	T1	18B	GND	NC	18C	RXD_B(10)	V3
19A	GND	NC	19B	RXCLK_B	V4	19C	GND	NC
20A	RXD_B(9)	R1	20B	N/A	U4	20C	RXD_B(8)	U3
21A	RXD_B(7)	P1	21B	N/A	T3	21C	RXD_B(6)	T2
22A	RXD_B(5)	N2	22B	N/A	R3	22C	RXD_B(4)	R2
23A	RXD_B(3)	M3	23B	N/A	P4	23C	RXD_B(2)	P3
24A	RXD_B(1)	M1	24B	N/A	N4	24C	RXD_B(0)	N3
25A	RXD_C(14)	L1	25B	RXERR_C	L2	25C	RXD_C(15)	L3
26A	RXD_C(12)	K1	26B	RXDVLOS_C	K4	26C	RXD_C(13)	K3
27A	RXD_C(10)	J1	27B	N/A	J5	27C	RXD_C(11)	J4
28A	RXD_C(8)	H1	28B	N/A	H4	28C	RXD_C(9)	H3
29A	RXD_C(6)	G1	29B	N/A	G3	29C	RXD_C(7)	G4
30A	GND	NC	30B	RXCLK_C	F3	30C	GND	NC
31A	RXD_C(4)	F1	31B	N/A	E3	31C	RXD_C(5)	F4
32A	RXD_C(2)	F2	32B	N/A	D1	32C	RXD_C(3)	E2
33A	RXD_C(0)	C1	33B	N/A	NC	33C	RXD_C(1)	D2
34A	VCC	NC	34B	VCC	NC	34C	VCC	NC
35A	VCC	NC	35B	VCC	NC	35C	VCC	NC
36A	VCC	NC	36B	VCC	NC	36C	VCC	NC
37A	RXD_D(14)	A4	37B	RXERR_D	B3	37C	RXD_D(15)	A3
38A	RXD_D(12)	A5	38B	RXDVLOS_D	C5	38C	RXD_D(13)	B4
39A	RXD_D(10)	B5	39B	N/A	D7	39C	RXD_D(11)	C7
40A	RXD_D(8)	B7	40B	N/A	B6	40C	RXD_D(9)	A6
41A	RXD_D(6)	A8	41B	N/A	E7	41C	RXD_D(7)	E8
42A	GND	NC	42B	RXCLK_D	D8	42C	GND	NC
43A	RXD_D(4)	B8	43B	N/A	E9	43C	RXD_D(5)	C8
44A	RXD_D(2)	A9	44B	N/A	D10	44C	RXD_D(3)	F9
45A	RXD_D(0)	B9	45B	N/A	NC	45C	RXD_D(1)	C10
46A	N/A	NC	46B	N/A	NC	46C	N/A	NC
47A	N/A	NC	47B		EXT_CLK_N	47C		EXT_CLK_P
48A	VAUX	NC	48B	VAUX	NC	48C	VAUX	NC