The Chimaera

Features

The back-end half of the board comprises one Spartan2e FPGA (xc2s200e), a flash memory (xc18v02) for non-volatile storage of the FPGA bitstream and one 256Mbit SDRAM. There is an on-board 80.44MHz crystal for those applications that require it.
The board is mechanically and electrically compatible with the S-link standard.
Power supplies are picked up either from mother board: +5V (raw, through S-link connector), Vaux (through auxiliary power pins SKT2). 2mm sockets for the 5V supply are also provided for standalone or testbench use. Vaux is not used by the back-end but is routed to the front-end coupling connector. There is no on-board over-voltage or reverse voltage protection.
The board implements a JTAG TAP for FPGA configuration.

FPGA configuration

Both the FPGA and its configuration flash memory are connected to the JTAG TAP. A bitstream may be directly loaded into the FPGA or downloaded into the flash memory from where it is downloaded to the FPGA on pressing SW1 or power cycling the board.

Connectors, switches and indicators

Program switch, SW1

SW1 triggers the reset of the FPGA. If “master serial” mode is selected and there is a valid bitstream in the configuration flash memory it is reloaded into the FPGA.

Configuration mode switch, SW2

SW2 is used to select between FPGA “boundary scan” or “master serial” configuration mode. The switch can normally be left in the “master serial” position as “boundary scan” (i.e. JTAG) configuration is also possible in this mode.

5V power and ground, TP1 and TP2

When not plugged into a motherboard it may be convenient to provide 5V power and ground to the board using these 2mm sockets.

Auxiliary power connector, SKT2

The S-link standard connector provides for only one power supply. For additional flexibility, socket SK2 is provided which mates with corresponding pins on the motherboard or can be connected to an auxiliary supply to provide an additional power voltage. The voltage can be any value and any polarity (it is not used on the back-end board) but must match the polarity requirements of the front-end half of the board to which it is connected through the front-end coupling connector.

S-link connector, PL1

This board is configured as an S-link LDC. The board can be used as a non-standard LSC provided care is taken with pin 5 of PL1. In standard usage pin 5 of an LDC is used for LDERR_B while for an LSC it is Vcc. Provided the FPGA IO J19 is not configured as a driver the board should also work as an LSC having J19 connected directly to Vcc. **If J19 is driving in this situation there is the possibility of signal contention which might result in permanent damage to the FPGA.**

Pin	Slink function	FPGA pin	Pin	Slink function	FPGA bin
1	LRL(3)	J17	2	LRL(2)	J18
3	VCC		4	LRL(1)	J20
5	LDERR_B/VCC	J19	6	LRL(0)	H19
7	LDOWN_B	H18	8	GND	
9	GND		10	LFF_B	G19
11	UCLK	G18	12	GND	
13	GND		14	UWEN_B	F20
15	URESET_B	F19	16	GND	
17	UDW(1)	D21	18	UTEST_B	E21
19	UCTRL_B	E19	20	UDW(0)	E20
21	UD(31)	B20	22	VCC	
23	GND		24	UD(30)	C21
25	UD(29)	A20	26	UD(28)	E15
27	UD(27)	B19	28	GND	
29	UD(26)	A19	30	UD(25)	E17
31	GND		32	UD(24)	C18
33	UD(23)	B18)	34	UD(22)	E16
35	UD(21)	A18	36	GND	
37	UD(20)	B17	38	UD(19)	C17
39	VCC		40	UD(18)	D16
41	UD(17)	A17	42	UD(16)	C16
43	UD(15)	B16	44	GND	
45	UD(14)	A16	46	UD(13)	D15
47	GND		48	UD(12)	C15
49	UD(11)	B15	50	UD(10)	D14
51	UD(9)	A15	52	VCC	
53	UD(8)	B14	54	UD(7)	C14
55	GND		56	UD(6)	D13
57	UD(5)	A14	58	UD(4)	C13
59	UD(3)	B13	60	GND	
61	UD(2)	A13	62	UD(1)	D12
63	VCC		64	UD(0)	C12

Front-end coupling connector, SKT1

The back-end board is normally connected to a front-end board. This connector provides power to the front-end board and links FPGA IO to signals on the front-end board. The signal names correspond to their function when used in conjunction with the Ophio front-end.

Pin	Ophio function	FPGA pin	Pin	Ophio function	FPGA pin	Pin	Ophio function	FPGA pin
1A	LED1A	U9	1B	LED1B	U10	1C	LED2A	V10
2A	LED2B	V11	2B	LED3A	W6	2C	LED3B	V9
3A	LED4A	AB11	3B	LED4B	AA6	3C	N/A	NC
4A	RXD(1)(15)	AB10	4B	RXERR(1)	W11	4C	RXD(1)(14)	Y11
5A	RXD(1)(13)	AA10	5B	RXDVLOS(1)	W10	5C	RXD(1)(12)	Y10
6A	RXD(1)(11)	AB9	6B	GND	NC	6C	RXD(1)(10)	Y9
7A	GND	NC	7B	RXCLK(1)	W9	7C	GND	NC
8A	RXD(1)(9)	AA9	8B	OPGND1	V8	8C	RXD(1)(8)	W9
9A	RXD(1)(7)	AB8	9B	RXPRBSEN(1)	V7	9C	RXD(1)(6)	W7
10A	RXD(1)(5)	AA8	10B	RXLCKREF_B(1)	AB5	10C	RXD(1)(4)	AB6
11A	RXD(1)(3)	AB7	11B	RXEN(1)	W5	11C	RXD(1)(2)	Y5
12A	RXD(1)(1)	AA7	12B	RXLOOPEN(1)	AA3	12C	RXD(1)(0)	AB3
13A	VCC	NC	13B	VCC	NC	13C	VCC	NC
14A	VCC	NC	14B	VCC	NC	14C	VCC	NC
15A	VCC	NC	15B	VCC	NC	15C	VCC	NC
16A	RXD(2)(15)	U2	16B	RXERR(2)	W3	16C	RXD(2)(14)	Y2
17A	RXD(2)(13)	U1	17B	RXDVLOS(2)	V2	17C	RXD(2)(12)	W1
18A	RXD(2)(11)	T1	18B	GND	NC	18C	RXD(2)(10)	V3
19A	GND	NC	19B	RXCLK(2)	V4	19C	GND	NC
20A	RXD(2)(9)	R1	20B	OPGND2	U4	20C	RXD(2)(8)	U3
21A	RXD(2)(7)	P1	21B	RXPRBSEN(2)	T3	21C	RXD(2)(6)	T2
22A	RXD(2)(5)	N2	22B	RXLCKREF_B(2)	R3	22C	RXD(2)(4)	R2
23A	RXD(2)(3)	M3	23B	RXEN(2)	P4	23C	RXD(2)(2)	P3
24A	RXD(2)(1)	M1	24B	RXLOOPEN(2)	N4	24C	RXD(2)(0)	N3
25A	RXD(3)(14)	L1	25B	RXERR(3)	L2	25C	RXD(3)(15)	L3
26A	RXD(3)(12)	K1	26B	RXDVLOS(3)	K4	26C	RXD(3)(13)	K3
27A	RXD(3)(10)	J1	27B	RXPRBSEN(3)	J5	27C	RXD(3)(11)	J4
28A	RXD(3)(8)	H1	28B	RXLCKREF_B(3)	H4	28C	RXD(3)(9)	H3
29A	RXD(3)(6)	G1	29B	OPGND3	G3	29C	RXD(3)(7)	G4
30A	GND	NC	30B	RXCLK(3)	F3	30C	GND	NC
31A	RXD(3)(4)	F1	31B	OPGND4	E3	31C	RXD(3)(5)	F4
32A	RXD(3)(2)	F2	32B	RXEN(3)	D1	32C	RXD(3)(3)	E2
33A	RXD(3)(0)	C1	33B	RXLOOPEN(3)	NC	33C	RXD(3)(1)	D2
34A	VCC	NC	34B	VCC	NC	34C	VCC	NC
35A	VCC	NC	35B	VCC	NC	35C	VCC	NC
36A	VCC	NC	36B	VCC	NC	36C	VCC	NC
37A	RXD(4)(14)	A4	37B	RXERR(4)	B3	37C	RXD(4)(15)	A3
38A	RXD(4)(12)	A5	38B	RXDVLOS(4)	C5	38C	RXD(4)(13)	B4
39A	RXD(4)(10)	B5	39B	RXPRBSEN(4)	D7	39C	RXD(4)(11)	C7
40A	RXD(4)(8)	B7	40B	RXLCKREF_B(4)	B6	40C	RXD(4)(9)	A6
41A	RXD(4)(6)	A8	41B	OPGND5	E7	41C	RXD(4)(7)	E8
42A	GND	NC	42B	RXCLK(4)	D8	42C	GND	NC
43A	RXD(4)(4)	B8	43B	OPGND6	E9	43C	RXD(4)(5)	C8
44A	RXD(4)(2)	A9	44B	RXEN(4)	D10	44C	RXD(4)(3)	F9
45A	RXD(4)(0)	B9	45B	RXLOOPEN(4)	NC	45C	RXD(4)(1)	C10
46A	N/A	NC	46B	N/A	NC	46C	N/A	NC
47A	N/A	NC	47B		FP_N	47C		FP_P
48A	VAUX	NC	48B	VAUX	NC	48C	VAUX	NC

Program indicator LED1

This LED normally lights briefly when PROGRAM is asserted (e.g. by pressing switch SW1).

Done indicator LED2

The LED normally lights when the FPGA is not configured (actually indicates NOT DONE). After successful configuration of the FPGA the LED should be off. The LED will remain on after pressing SW1 if the FPGA is in “boundary scan” configuration mode and the bitstream has not yet been downloaded or in “master serial” mode if there is no valid bitstream in the configuration flash memory.

USB interface

The Chimaera can be used in combination with a USB adapter to provide a convenient interface to a PC where the higher bandwidth provided by the S-link is not required. The USB interface couples to the Chimaera using socket PL1 so USB and S-link usage are mutually exclusive. Furthermore, the Chimaera must be loaded with the appropriate firmware. **Using incorrect firmware may result in signal contention and consequential damage.** The USB interface allows a more flexible bidirectional interface to the Chimaera than is possible with the simplex S-link.

The USB adapter is based on the Silicon Laboratories C8051F32x MCU. Communication between Chimaera, the USB MCU, and the host PC uses a simple message-passing protocol based on the USBXpress driver and device and host API.