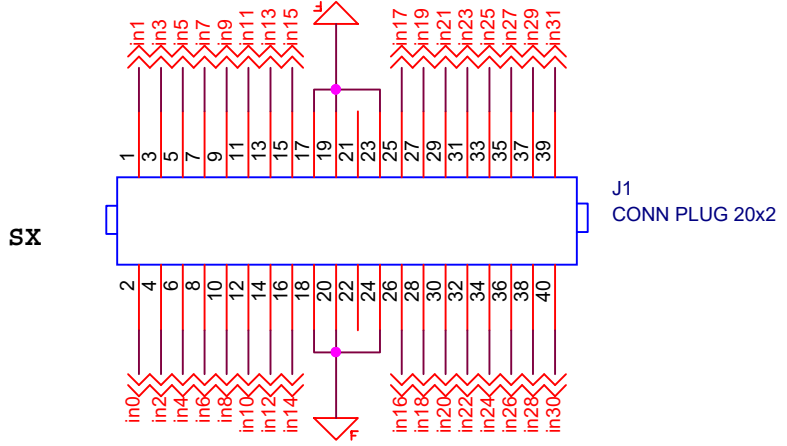
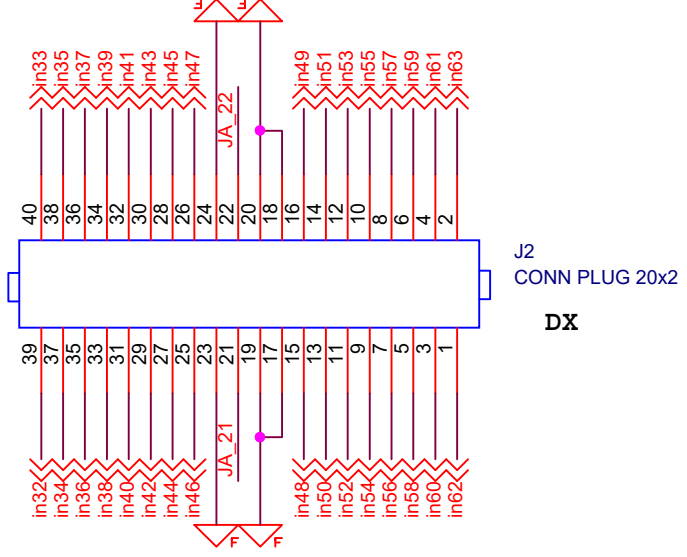


LAYER TOP



LAYER BOTTOM

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23/07/14 Aggiunta pagina per Note.

23/07/14 Inseirte induttanze in serie all'alimentazione. Schema versione 2_2

28/07/14 Inseirta resistenza da 22ohm in serie a ciscun MOSI. Schema versione 2_3 (master V2-5)

15/10/14 Scambiato Avdd e GND nei collegamenti di R31 e C47. Schema versione 2_4 (stesso master V2-5)

20/03/2015 Schema versione 2_7. Con resistenze anti-oscillazione in serie alle uscite.
Senza buffer dei primi due canali di uscita. (master V2_7)

23/03/15 Scambiati Gate A/B di U17 per semplificare il routing

07/04/15 Aggiornato pin-out con CLARO8V2. Aggiunte resistenze di collegamento linee nPOR.
Tolte resitenze su MOSI, Collegato Config_WR_EN. (Master V2-7.2)

26/06/2015 ho notato che il pcbFootprint del connettore J3 ha il nome del connettore femmina posto sulla scheda PDM-BackBoard.
Il nome e' sbagliato ma il componente e' disegnato correttamente.

01/12/15 VERSIONE3

Rimossi i componenti attivi, aggiunte resistenze in serie alle alimentazioni,
"separate" le masse degli ingressi dalle masse delle uscite.

La linea nSEL diventa FEB-enable e collega assieme tutti i Chain-En.
Le 8 linee Chain_En diventano gli nSEL dei singoli CLARO.

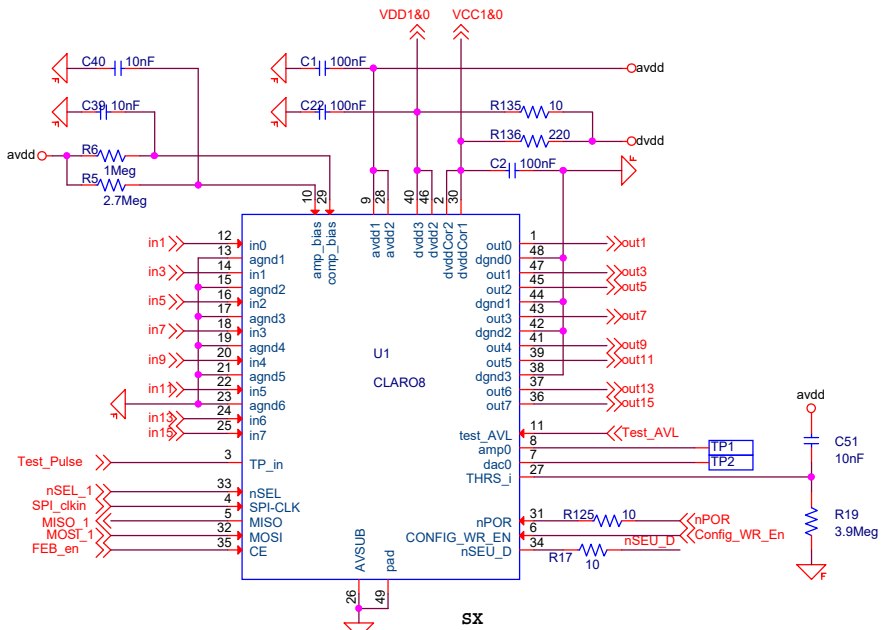
modificati valori delle resistenze di polarizzazione: 2.7M iamp, 1M icomp, 3.9M ithresh

Per motivi di spazio tolte le 8 resistenze da zero Ohm in serie a AVDD

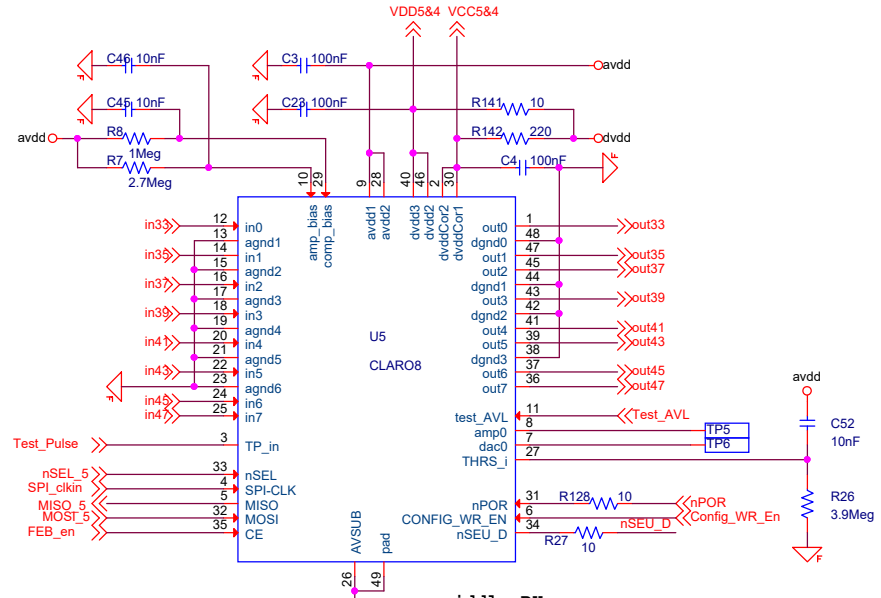
Aggiunto condensatore su AVL; aggiunta terminazione su linea SPICLK; Aggiunta PT1000 in 1206

25/02/16 aggiunte resistenze R48, R49, R50, R51 per monitor Vcore; collegate su pin J3.56

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Note		
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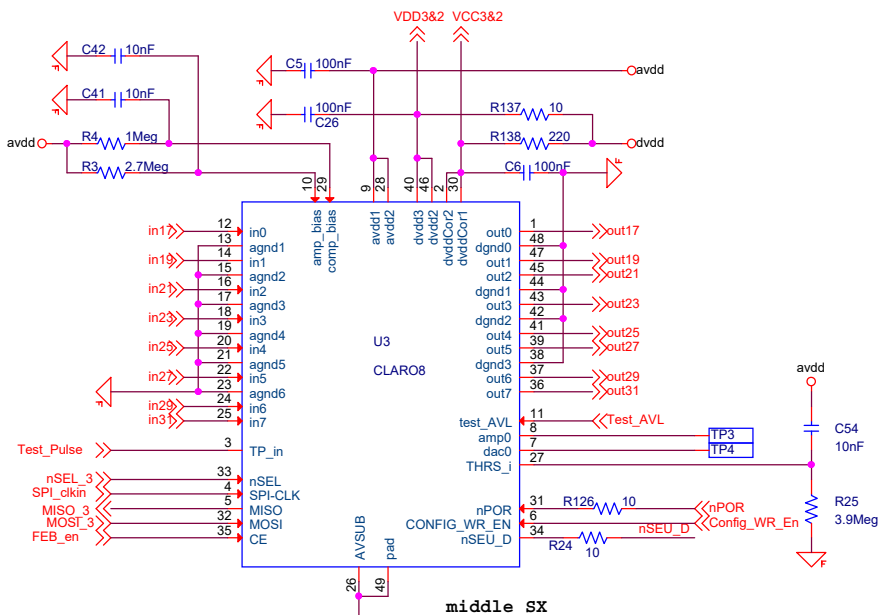


SX

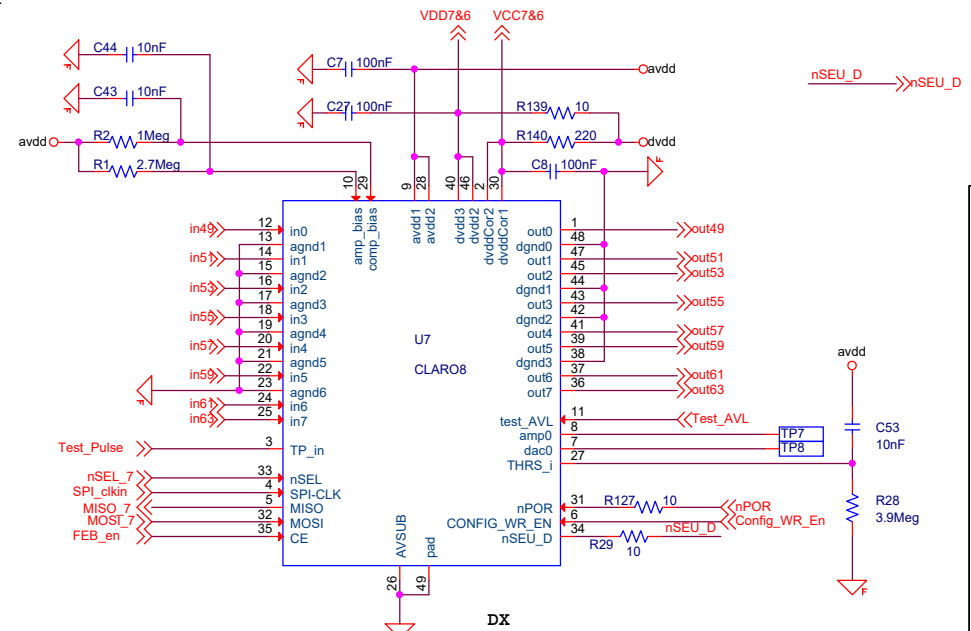


middle DX

LATO TOP

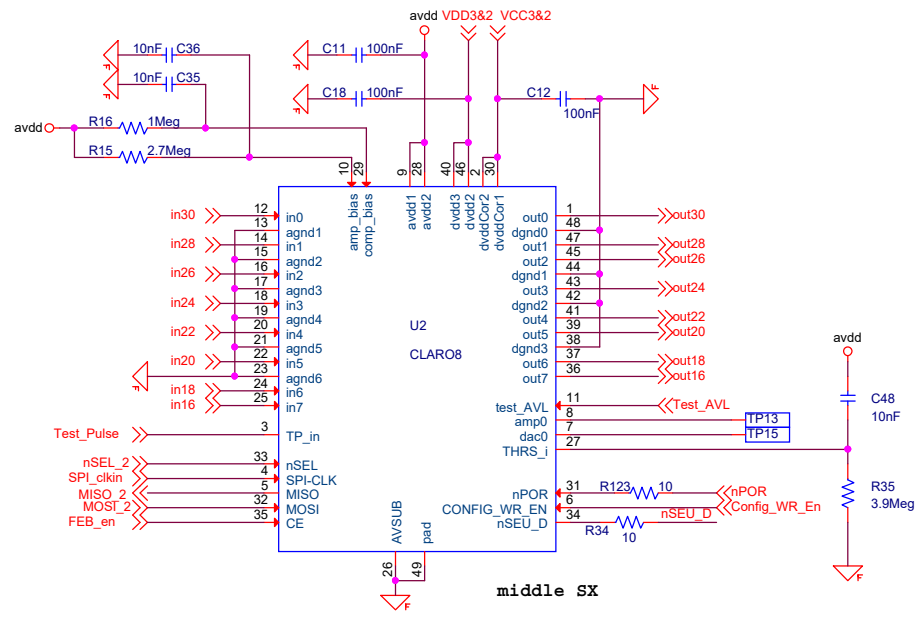
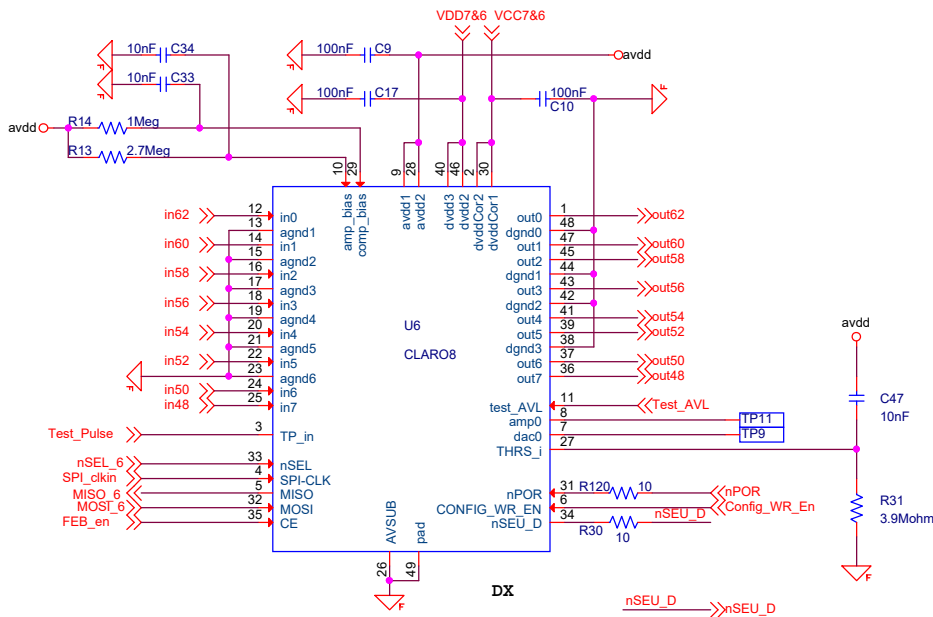


middle SX

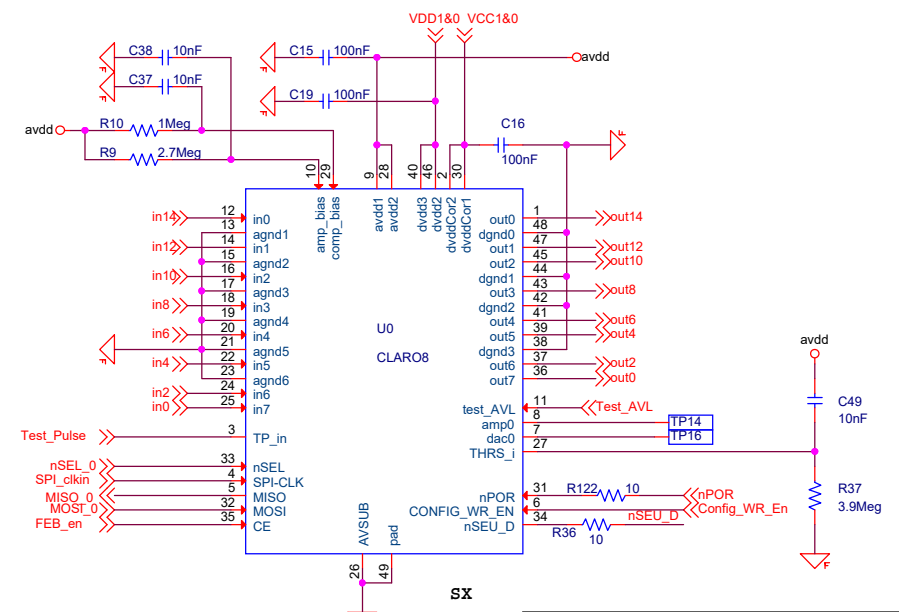
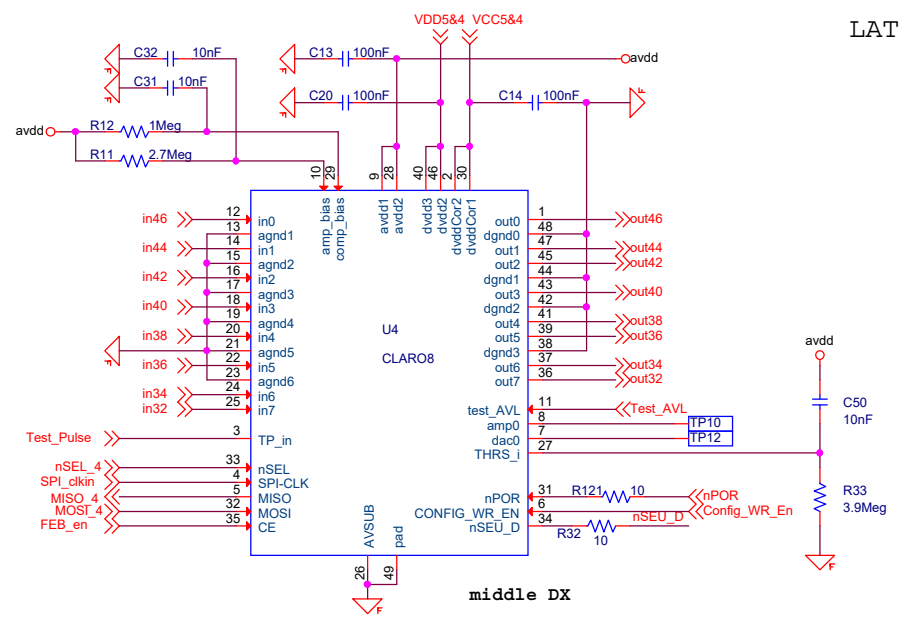


DX

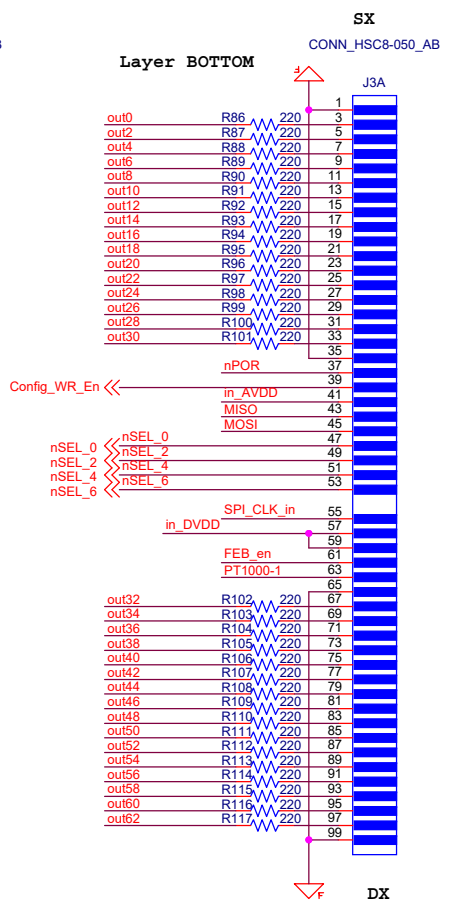
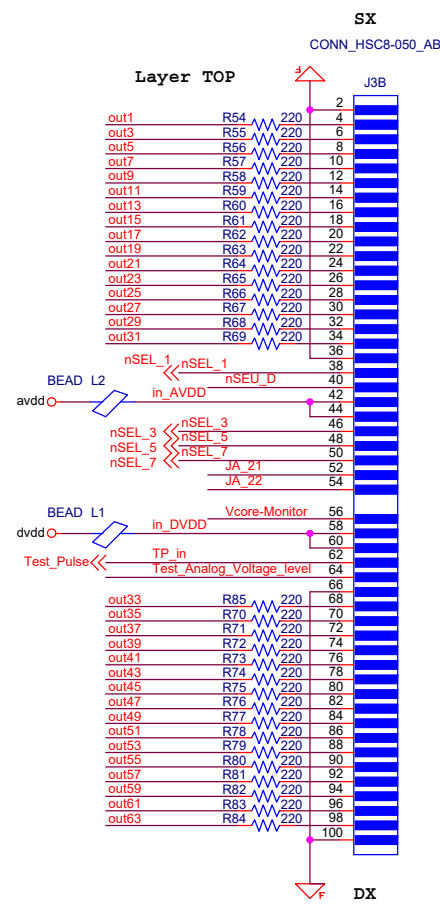
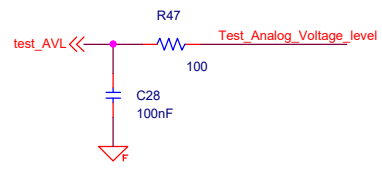
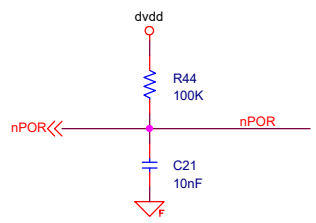
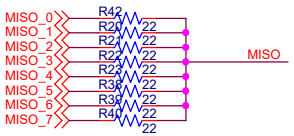
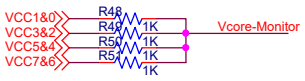
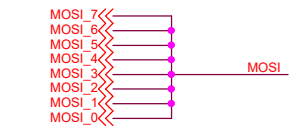
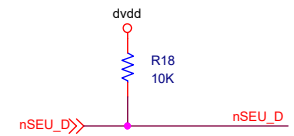
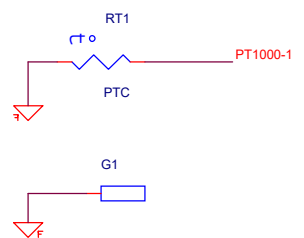
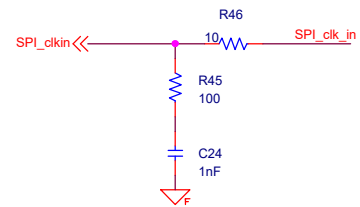
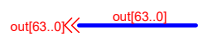
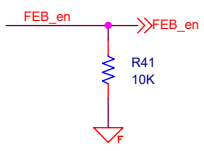
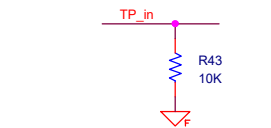
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