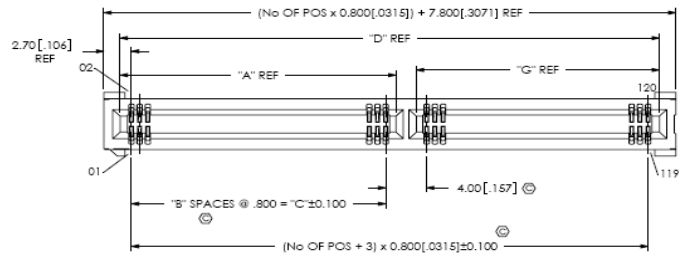
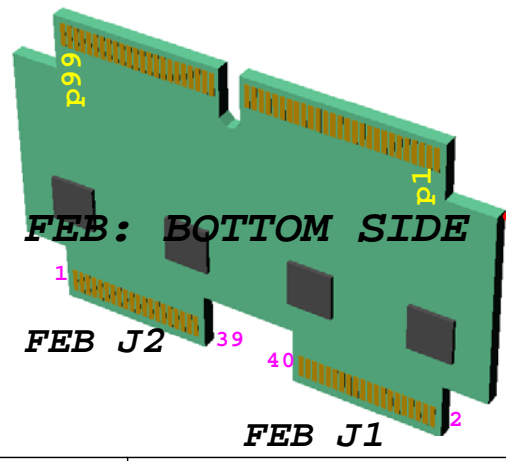


BASEBOARD (VIEW FROM PMT SIDE)

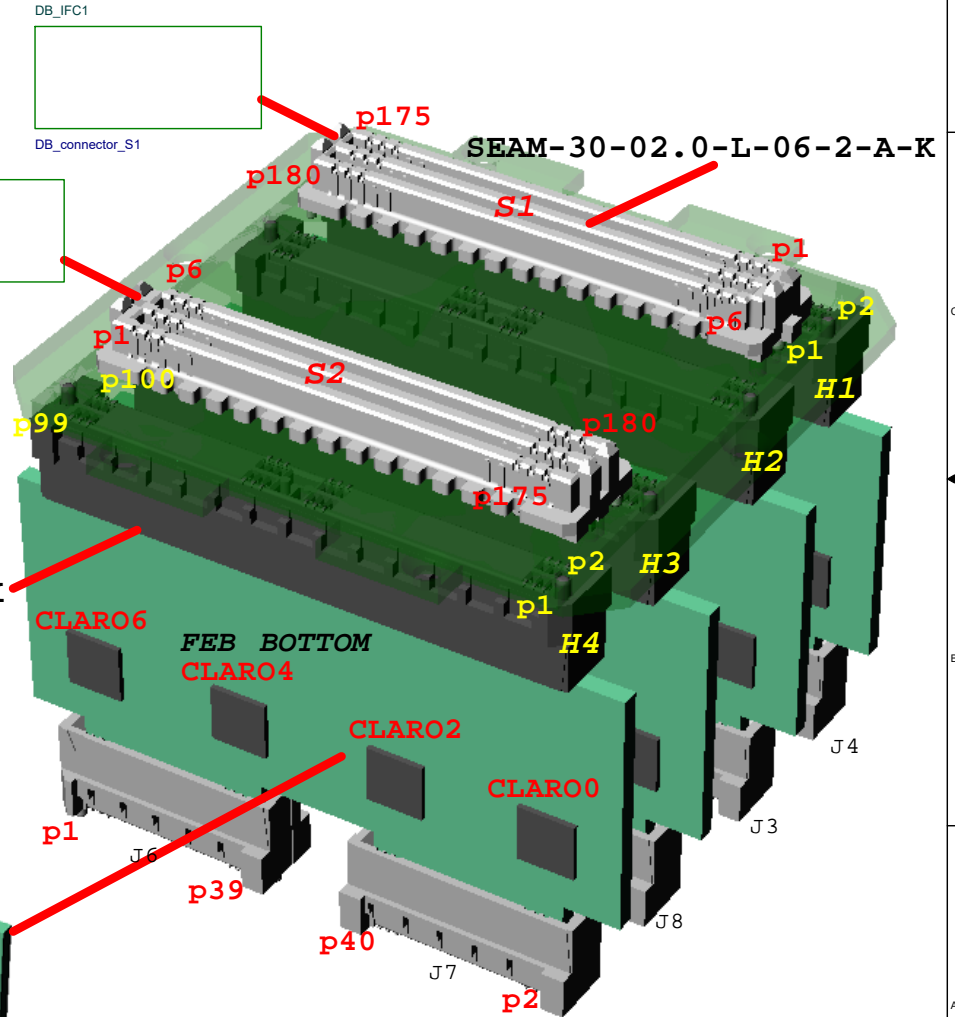
PT1000_A
PT1000_B



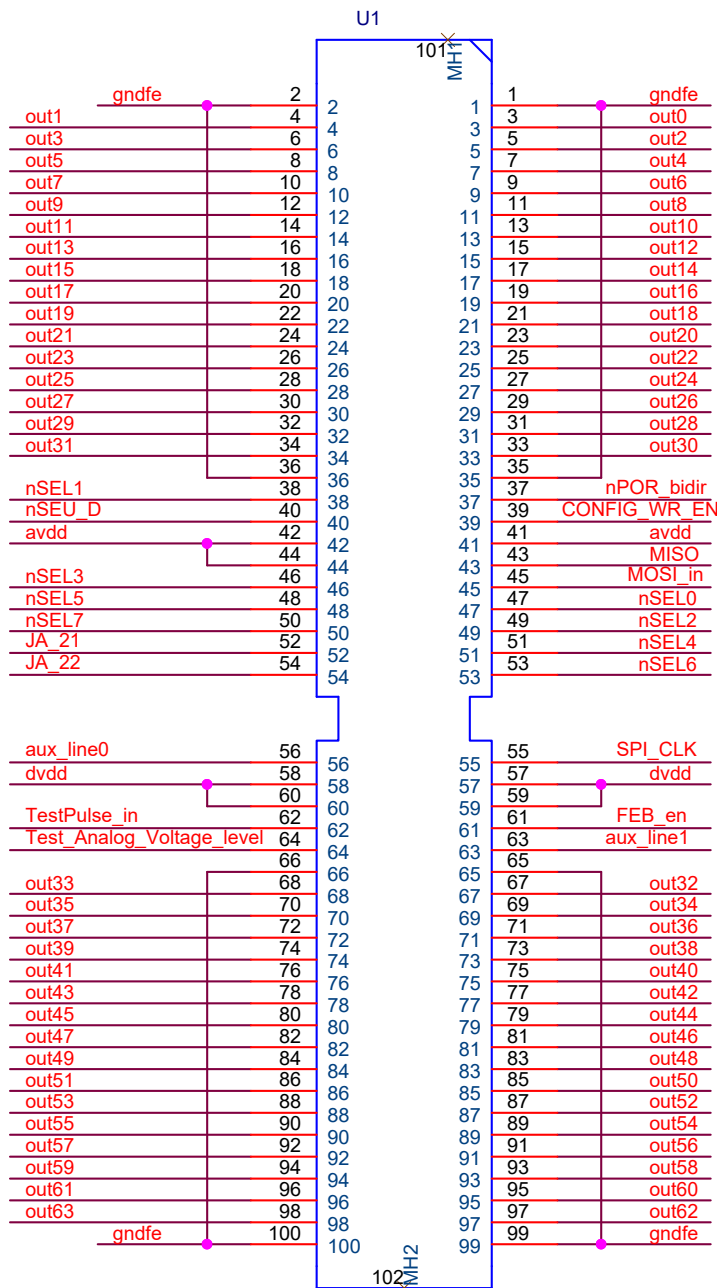
HSEC8_150_01_L_DV_A_K



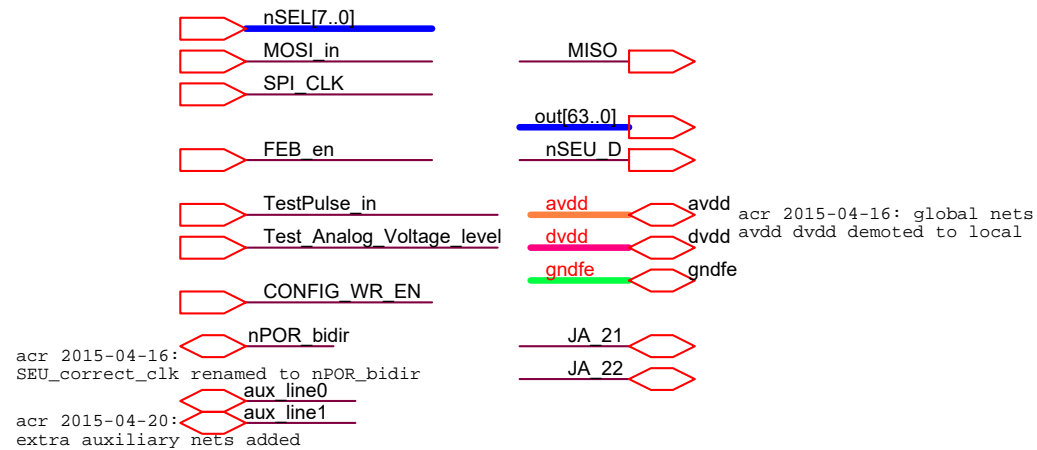
FEB: BOTTOM SIDE



INFN-Ferrara / INFN Milano-Bicocca		
Title Elementary Cell's (EC) backboard designer: Angelo Cotta Ramusino		
Size B	Document Number BB_sch_main	Rev 2.0
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HSEC8_150_01_L_DV_A_K

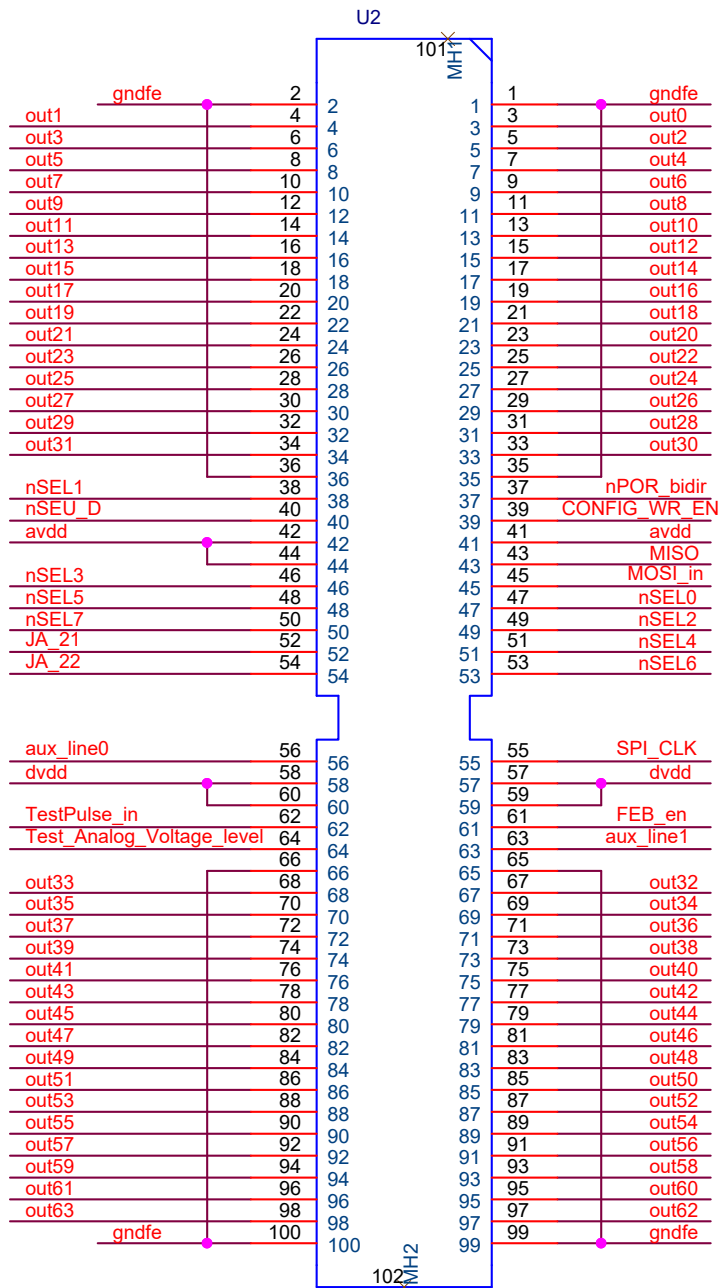


N.B.:

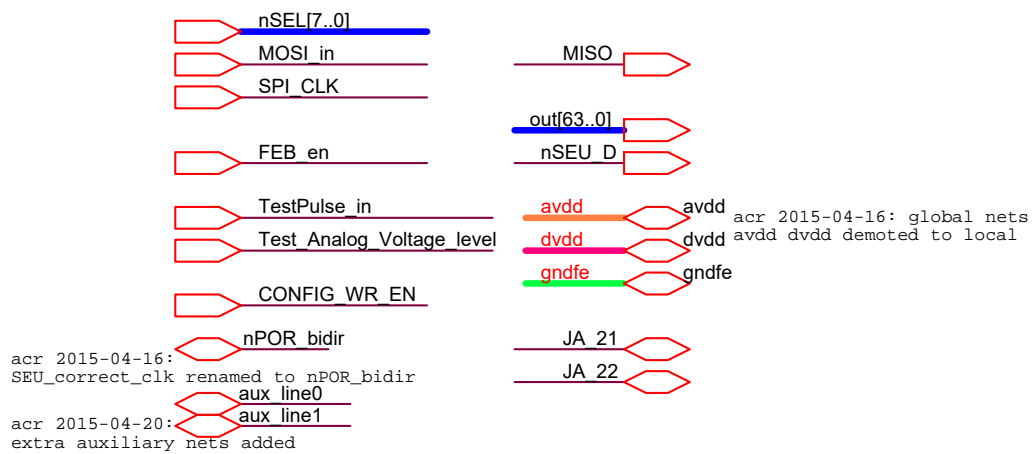
- 1) in this version the nSEL[7..0] lines from the GBT-SCA are routed to the nSEL input of the 8 CLAROS and a single "FEB_en" signal is routed to all the "CHAIN_ENABLE" input of the CLAROS
- 2) the "aux_line1..0" could be used to connect a PT1000 located on the FEB unless needed for power down control

history of mods:
 acr 20160105 renamed:
 * SEU_D to nSEU_D
 * Chain_En[7..0] to nSEL[7..0]
 * nSEL_in to FEB_en

 INFN-Ferrara / INFN Milano-Bicocca	
Title Photo Detector Module's backboard designer: Angelo Cotta Ramusino	
Size A	Document Number backboard_to_FEB_interface
Rev 2.0	
Date: Monday, February 29, 2016	
Sheet 2	of 7




HSEC8_150_01_L_DV_A_K

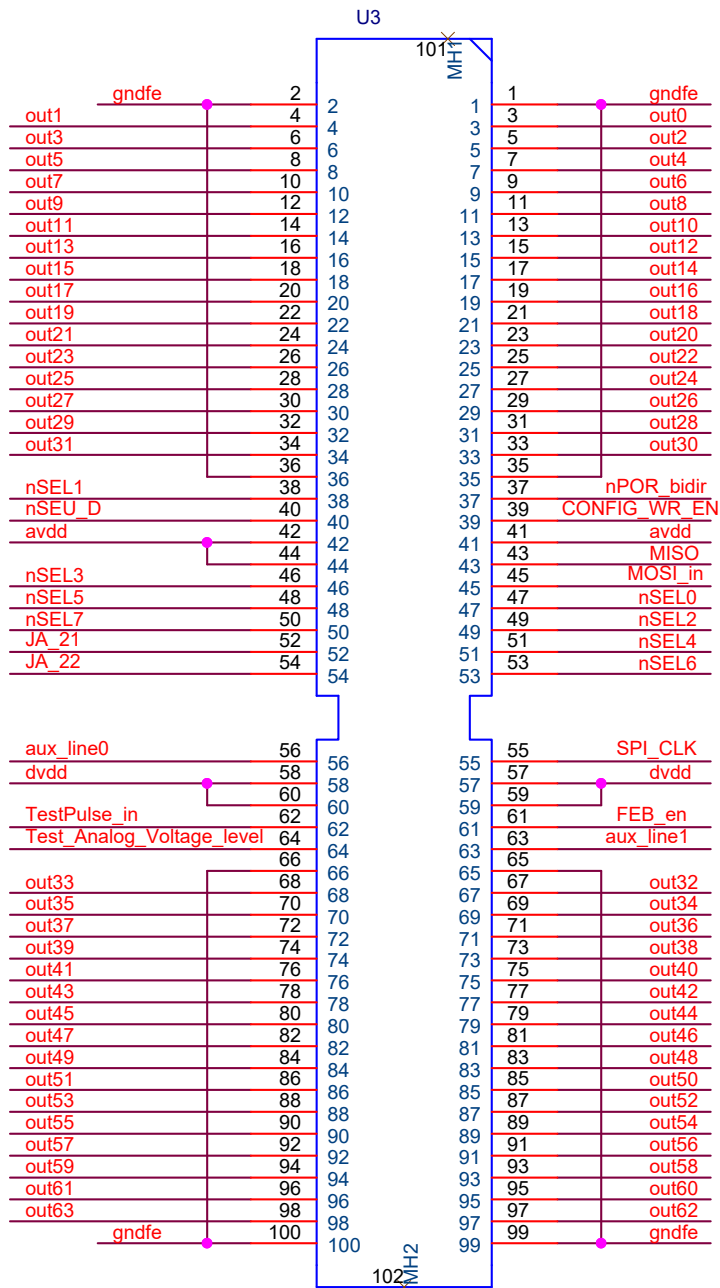


N.B.:

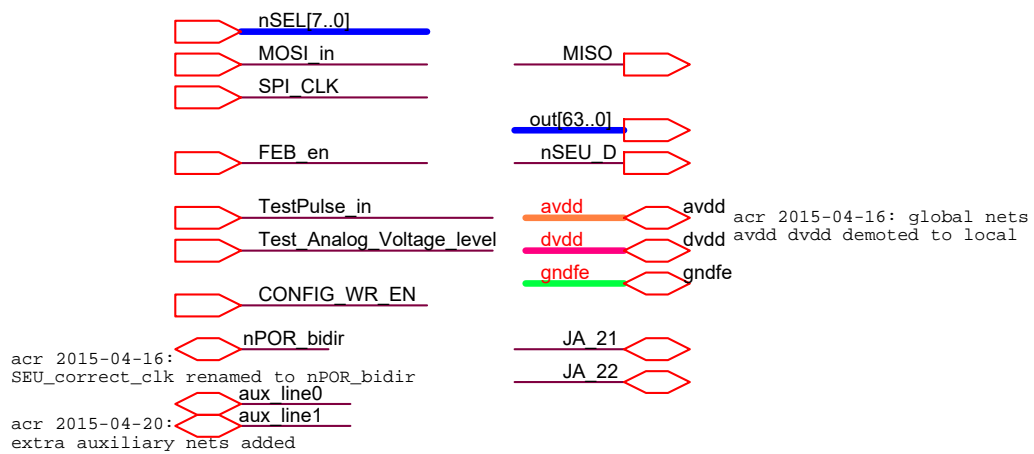
- 1) in this version the nSEL[7..0] lines from the GBT-SCA are routed to the nSEL input of the 8 CLAROS and a single "FEB_en" signal is routed to all the "CHAIN_ENABLE" input of the CLAROS
- 2) the "aux_line1..0" could be used to connect a PT1000 located on the FEB unless needed for power down control

history of mods:
 acr 20160105 renamed:
 * SEU_D to nSEU_D
 * Chain_En[7..0] to nSEL[7..0]
 * nSEL_in to FEB_en

 INFN-Ferrara / INFN Milano-Bicocca	
Title Photo Detector Module's backboard designer: Angelo Cotta Ramusino	
Size A	Document Number backboard_to_FEB_interface
Date: Monday, February 29, 2016	Rev 1.0 Sheet 3 of 7




HSEC8_150_01_L_DV_A_K

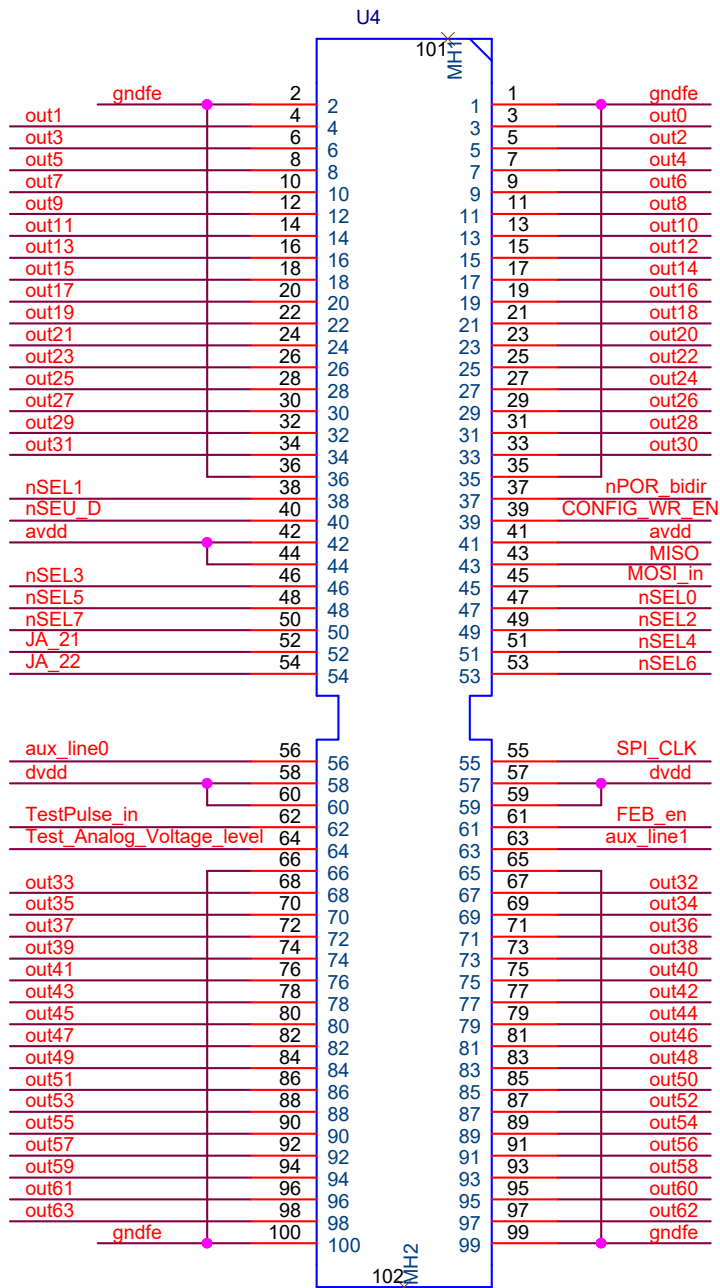


N.B.:

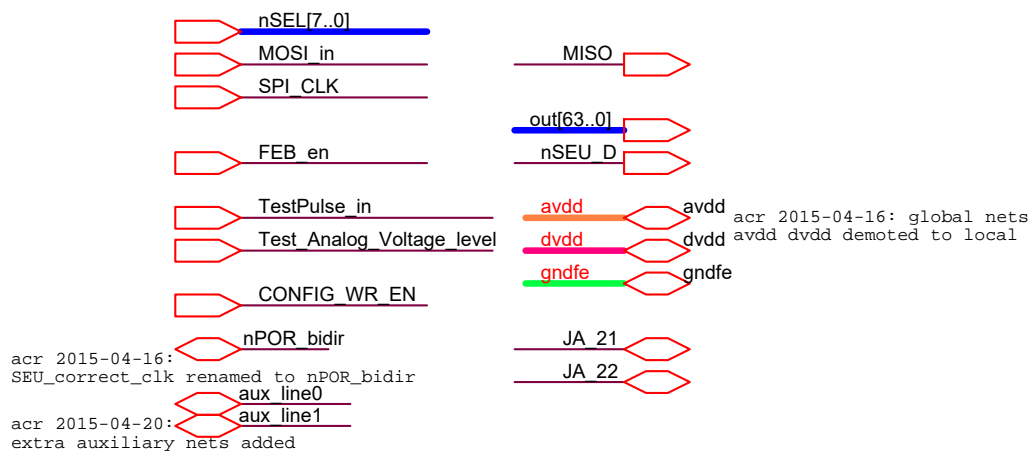
- 1) in this version the nSEL[7..0] lines from the GBT-SCA are routed to the nSEL input of the 8 CLAROS and a single "FEB_en" signal is routed to all the "CHAIN_ENABLE" input of the CLAROS
- 2) the "aux_line1..0" could be used to connect a PT1000 located on the FEB unless needed for power down control

history of mods:
 acr 20160105 renamed:
 * SEU_D to nSEU_D
 * Chain_En[7..0] to nSEL[7..0]
 * nSEL_in to FEB_en

 INFN-Ferrara / INFN Milano-Bicocca	
Title Photo Detector Module's backboard designer: Angelo Cotta Ramusino	
Size A	Document Number backboard_to_FEB_interface
Date: Monday, February 29, 2016	Rev 1.0
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HSEC8_150_01_L_DV_A_K

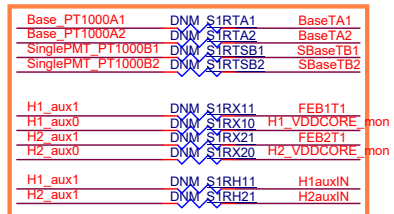
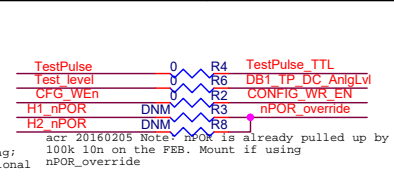
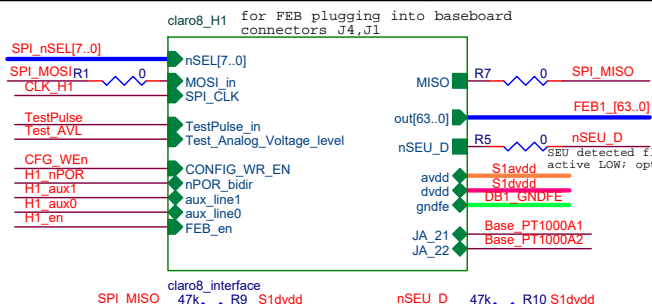


N.B.:

- 1) in this version the nSEL[7..0] lines from the GBT-SCA are routed to the nSEL input of the 8 CLAROS and a single "FEB_en" signal is routed to all the "CHAIN_ENABLE" input of the CLAROS
- 2) the "aux_line1..0" could be used to connect a PT1000 located on the FEB unless needed for power down control

history of mods:
 acr 20160105 renamed:
 * SEU_D to nSEU_D
 * Chain_En[7..0] to nSEL[7..0]
 * nSEL_in to FEB_en

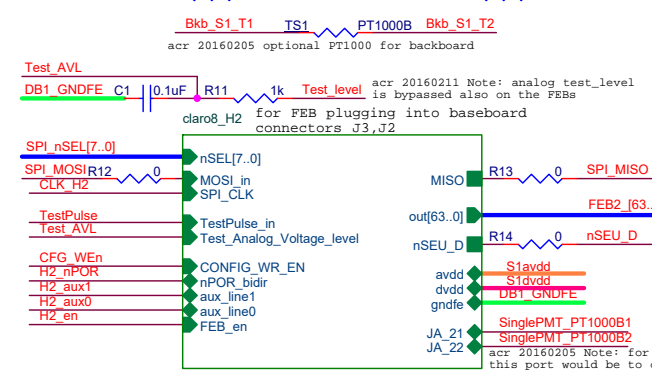
		INFN-Ferrara / INFN Milano-Bicocca	
Title			
Photo Detector Module's backboard			
designer: Angelo Cotta Ramusino			
Size	Document Number		Rev
A	backboard_to_FEB_interface		2.0
Date:	Monday, February 29, 2016	Sheet	5 of 7



FEB1_2	1	S1A
FEB1_4	7	1
FEB1_6	13	1
FEB1_8	19	1
FEB1_10	25	1
FEB1_12	31	1
FEB1_14	37	1
FEB1_16	43	1
FEB1_18	49	1
FEB1_20	55	1
FEB1_22	61	1
FEB1_24	67	1
FEB1_26	73	1
FEB1_28	79	1
FEB1_30	85	1
FEB1_32	91	1
FEB1_34	97	1
FEB1_36	103	1
FEB1_38	109	1
FEB1_40	115	1
FEB1_42	121	1
FEB1_44	127	1
FEB1_46	133	1
FEB1_48	139	1
FEB1_50	145	1
FEB1_52	151	1
FEB1_54	157	1
FEB1_56	163	1
FEB1_58	169	1
FEB1_60	175	1

FEB1_3	2	S1B
FEB1_5	8	2
FEB1_7	14	2
FEB1_9	20	2
FEB1_11	26	2
FEB1_13	32	2
FEB1_15	38	2
FEB1_17	44	2
FEB1_19	50	2
FEB1_21	56	2
FEB1_23	62	2
FEB1_25	68	2
FEB1_27	74	2
FEB1_29	80	2
FEB1_31	86	2
FEB1_33	92	2
FEB1_35	98	2
FEB1_37	104	2
FEB1_39	110	2
FEB1_41	116	2
FEB1_43	122	2
FEB1_45	128	2
FEB1_47	134	2
FEB1_49	140	2
FEB1_51	146	2
FEB1_53	152	2
FEB1_55	158	2
FEB1_57	164	2
FEB1_59	170	2
FEB1_61	176	2

FEB1_1	3	S1C
FEB1_0	9	3
DB1_GNDFE	15	3
SPI_MISO	21	3
nSEU_D	27	3
Bkb_S1_T1	33	3
CONFIG_WR_EN	39	3
BaseTA1	45	3
SBaseTB1	51	3
DB1_GNDFE	57	3
nPOR_override	63	3
SPI_CLK	69	3
SPI_MOSI	75	3
DB1_GNDFE	81	3
DB1_I2C_SDA	87	3
DB1_I2C_SCL	93	3
H1_en	99	3
H2_en	105	3
DB1_GNDFE	111	3
DB1_VDDFE	117	3
FEB1T1	123	3
FEB2T1	129	3
H1auxIN	135	3
DB1_VDDFE	141	3
TestPulse_TTL	147	3
ALDO_IFC1_En	153	3
DB1_GNDFE	159	3
FEB1_62	165	3
FEB1_63	171	3



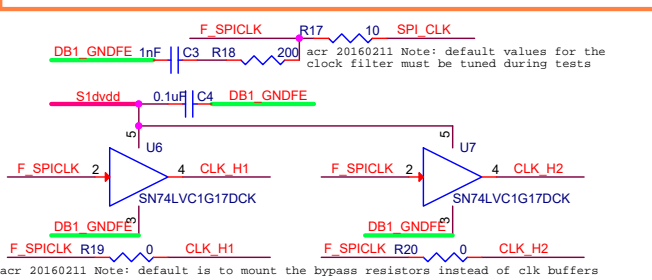
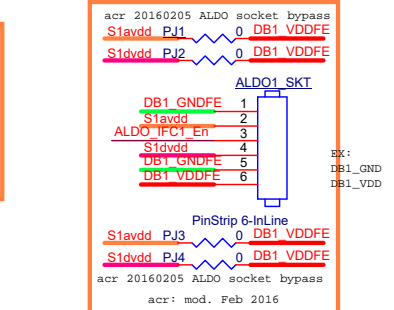
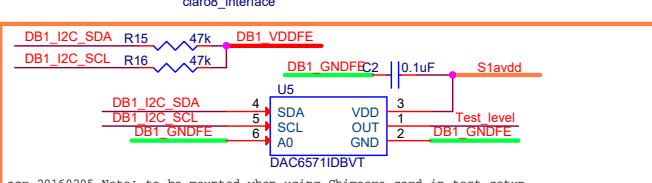
acr 20160208 Note: NOT to be mounted when using Chimera card in test setup

acr 20160208 Note: H1aux1..0 and H2aux1..0 are connected to PT1000 or to resources for SEL detection

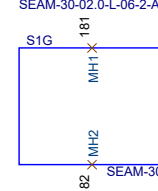
FEB2_1	4	S1D
FEB2_0	10	4
DB1_GNDFE	16	4
DB1_TP_DC_AnlgLv	22	4
Bkb_S1_T2	28	4
BaseTA2	34	4
SBaseTB2	40	4
DB1_GNDFE	46	4
SPI_nSEL0	52	4
SPI_nSEL1	58	4
SPI_nSEL2	64	4
SPI_nSEL3	70	4
DB1_GNDFE	76	4
SPI_nSEL4	82	4
SPI_nSEL5	88	4
SPI_nSEL6	94	4
SPI_nSEL7	100	4
DB1_GNDFE	106	4
DB1_VDDFE	112	4
H1_VDDCORE_mon	118	4
H2_VDDCORE_mon	124	4
H2auxIN	130	4
DB1_VDDFE	136	4
DB1_VDDFE	142	4
DB1_VDDFE	148	4
DB1_VDDFE	154	4
DB1_VDDFE	160	4
DB1_GNDFE	166	4
FEB2_62	172	4
FEB2_63	178	4

FEB2_2	5	S1E
FEB2_4	11	5
FEB2_6	17	5
FEB2_8	23	5
FEB2_10	29	5
FEB2_12	35	5
FEB2_14	41	5
FEB2_16	47	5
FEB2_18	53	5
FEB2_20	59	5
FEB2_22	65	5
FEB2_24	71	5
FEB2_26	77	5
FEB2_28	83	5
FEB2_30	89	5
FEB2_32	95	5
FEB2_34	101	5
FEB2_36	107	5
FEB2_38	113	5
FEB2_40	119	5
FEB2_42	125	5
FEB2_44	131	5
FEB2_46	137	5
FEB2_48	143	5
FEB2_50	149	5
FEB2_52	155	5
FEB2_54	161	5
FEB2_56	167	5
FEB2_58	173	5
FEB2_60	179	5

FEB2_3	6	S1F
FEB2_5	12	6
FEB2_7	18	6
FEB2_9	24	6
FEB2_11	30	6
FEB2_13	36	6
FEB2_15	42	6
FEB2_17	48	6
FEB2_19	54	6
FEB2_21	60	6
FEB2_23	66	6
FEB2_25	72	6
FEB2_27	78	6
FEB2_29	84	6
FEB2_31	90	6
FEB2_33	96	6
FEB2_35	102	6
FEB2_37	108	6
FEB2_39	114	6
FEB2_41	120	6
FEB2_43	126	6
FEB2_45	132	6
FEB2_47	138	6
FEB2_49	144	6
FEB2_51	150	6
FEB2_53	156	6
FEB2_55	162	6
FEB2_57	168	6
FEB2_59	174	6
FEB2_61	180	6



acr 2016-02-24:
 signals H1_VDDCORE_mon and H2_VDDCORE_mon may be "added" through "mixing" resistor RMIX.
 The voltage ranges of signals H1_VDDCORE_mon and H2_VDDCORE_mon are adjusted (separately or jointly) to the GBT-SCA ADC MAX input voltage through RDIV_H1 and RDIV_H2 (and of course S1RX10 and S1RX20)



INFN-Ferrara / INFN Milano-Bicocca

Title: Photo Detector Module's backboard
 designer: A. Cotta Ramusino, C. Gotti

Size B Document Number: DB_Interface_1 Rev 2.0

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