

>> Data Fibres <<

LVDS
Data Streams x12

DFbr 0
DFbr 1
DFbr 2
DFbr 3

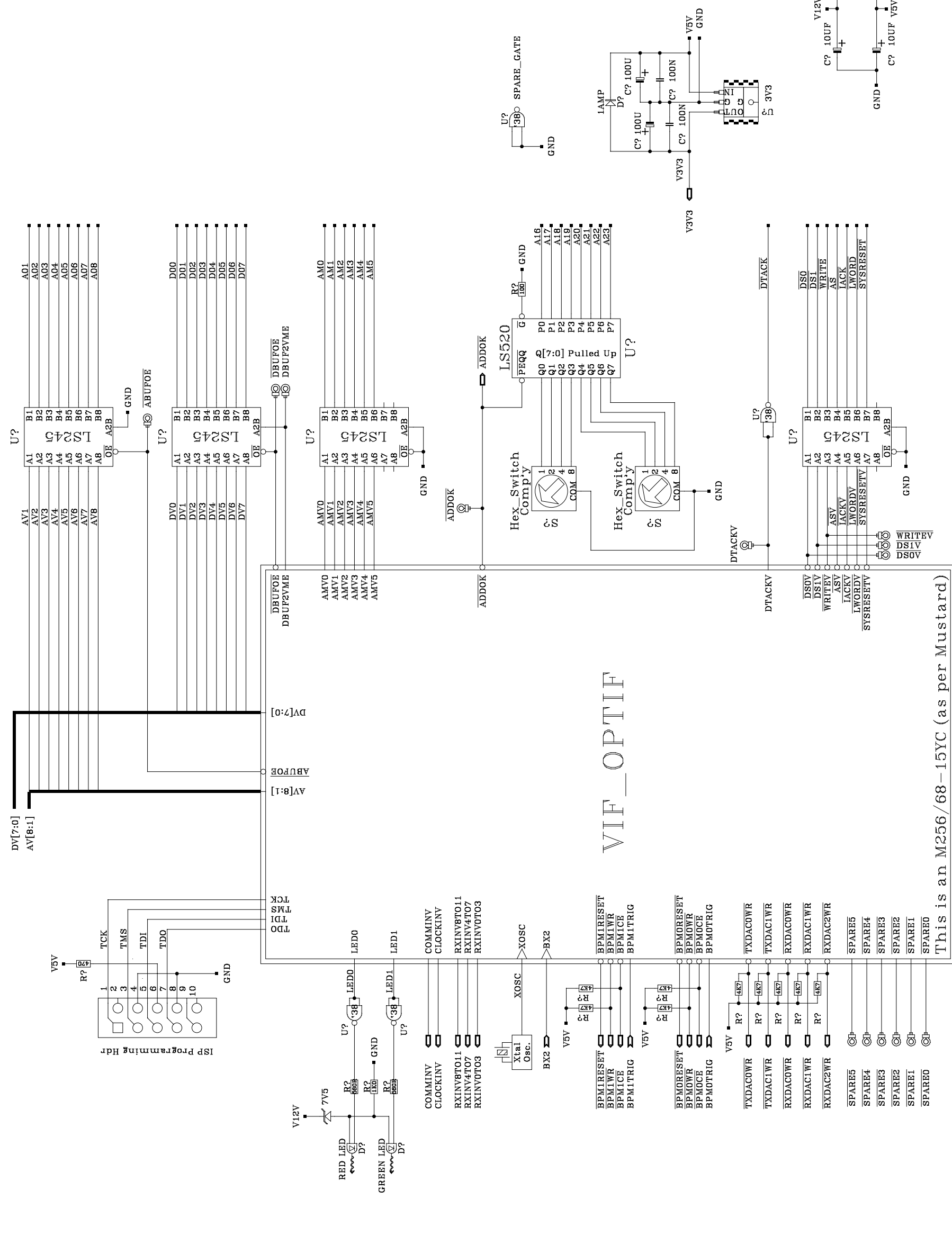
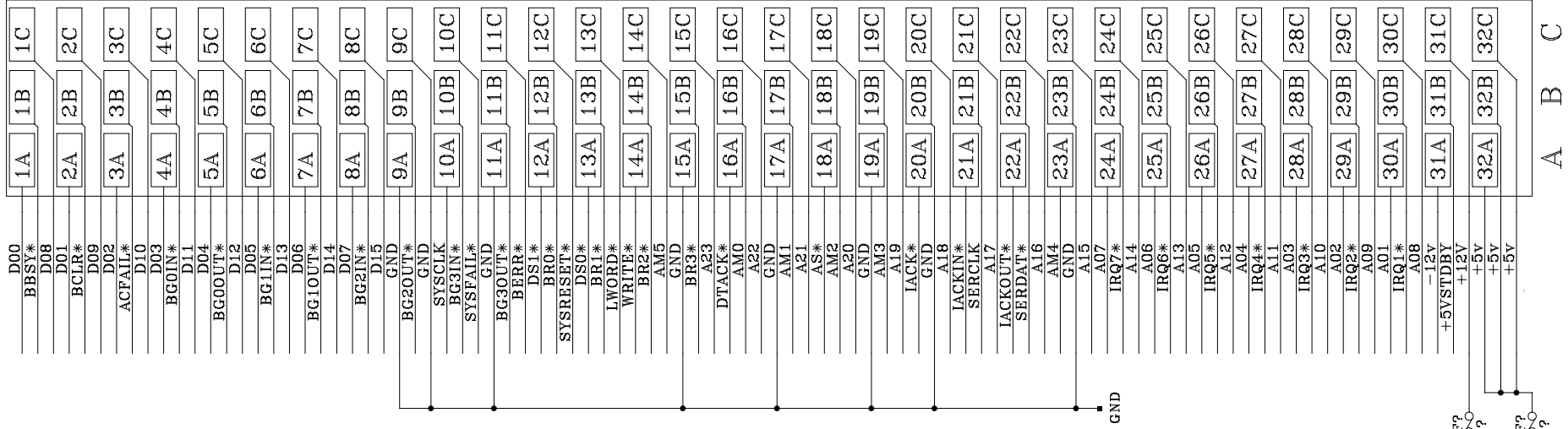
DFbr 4
DFbr 5
DFbr 6
DFbr 7

DFbr 8
DFbr 9
DFbr 10
DFbr 11

Dstr 11
Dstr 10
Dstr 9
Dstr 8
Dstr 7
Dstr 6
Dstr 5
Dstr 4
Dstr 3
Dstr 2
Dstr 1
Dstr 0

V3V3
V5V
V12V

RXINV8TO11
RXINV4TO7
RXINV0TO3



This is an M256/68-15YC (as per Mustard)

OptIF_Notes

- 1) DRX Pinout ... W/B 12 July from DW
- 2) DRX: 3v3 CLCC28 (j-lead)
- 3) DRX T/Hold: 0-240uA (sink) for I/P 0-2v4 (10K to 2v4)
- 4) BPM I_Laser I/Ps (VBias): 1K to 0.7v, x10 scaling
- 5) BPM: Clock I/P is PECL: others are CMOS ??
- 6) Lots of decouplers: layout round the BPMs/lasers needs careful thought
- 7) Scope Ground bars as per Mustard, please
- 8) Xtal Osc: RS 226-2294 (8MHz, SMT)
- 9) Hex_Sw_Complementary is Farnell part 146-199
- 10) Mount Hex Switches with window to front
- 11) LVDS Line terminations all 100R
- 12) VME Connector .. prefer reversed symbol
- 13) Quad DACs AD7305 or MAX506 .. but diff conn's
- 14) OpAmps ??? ... Dual or SOT23 singles ???
- 15) LS682 possible alternative to LS520: omit R1
- 16) VPin?? ... zener and series R TBD
- 17) VME I/F Pinout: could choose pinout to suit layout, then try to fit
- 18) PIN Array: 4D470 on carrier: awaiting pinout
- 19) VCSEL Array (if used): 4D469 on carrier: awaiting pinout
- 20) Devices: sn74F38, mc10ELT20, ds90LV047, ds90LV048
- 21) Single VCSELS: hfe4080-321
- 22) Laser interlock microswitches on sub assembly (TBD)
- 23) 3v3 3-terminal regulator: BA033T used on Mustard
- 23) Must have at least one LED

Mod's Record (key mod's only)

Date	Sheet	Description
06-Jul-1999	1	BPM pinout corrected (Address pins reversed)
06-Jul-1999	1	PECL termination changed (BPM clock inputs)
07-Jul-1999	1&2	DAC address lines >> AV[2:1]
07-Jul-1999	1&2	PullUp added to DAC A0/SHDN pin (preventing sleep mode)
07-Jul-1999	3	Add 3v3 regulator & associated comp's
07-Jul-1999	3	74f38 spare gate I/P's grounded
07-Jul-1999	1&3	LED added
07-Jul-1999	1,2&3	Changed DAC & signal names to RXDAC.. & TXDAC..
07-Jul-1999	1,2&3	DAC LDAC pins fixed low
07-Jul-1999	1&3	Address connections widened to A[8:1]
07-Jul-1999	1&2	LVDS LV chip pullups go to 3v3v (not v5v)
12-Jul-1999	1	Second LED added (why not)
12-Jul-1999	1	10K bleed resistors added to laser anode circuits
12-Jul-1999	1	VOUTD wiring error corrected (DAC0)
12-Jul-1999	1	Spare HCT inputs strapped to CLOCKINY
12-Jul-1999	1	EX3 TestPoint added
12-Jul-1999	2	Missing GND connection to RXDAC zeners added
12-Jul-1999	3	TestPoints added to spare MACH I/Os
13-Jul-1999	3	MACH ISP header pin 6 pullup to V5V (not VDD5) .. value added
13-Jul-1999	3	Pullups added to BPM and DAC control lines (switch-on)
14-Jul-1999	1	LED's removed from this sheet (see sheet 3)
14-Jul-1999	3	LEDs added, circuit modified