B-Layer Notes:

**Pixel Requirements (Provisional):**

0) 1 Clock and Control fibre per module

1) 2 Data fibres per module: the data is split into 4-bit nibbles by the MCC: bits 0 and 2 are time multiplexed onto one fibre, and bits 1 and 3 onto the other. The first bit of a data packet always appears as bit 0. Each data fibre carries 80 MBit/s data, giving an aggregate data rate of 160 MBit/s per Pixel module.

2) 6 or 7 modules per BOC/ROD

3) all fibres connect as 8-way ribbons: 1 Clock and Control ribbon, and 2 Data ribbons

**BOC and ROD Loading:**

0) BOC needs only 1 Opto-TX card loaded in location OTX0

1) ROD needs only serve Clock and Control streams [9:2]

2) BOC has only 2 Opto-RX cards loaded in locations ORX0 and ORX4

3) BOC needs only PHOS4 Data Delay chips for BOC streams [11:0] and [59:48] (i.e. 6 PHOS4s)

4) BOC has only 2 RX-PLDs loaded, RX-PLDO and RX-PLD2

5) ROD has only 4 Formatters loaded in locations [0,1,4,5]

6) BOC loading may be more than the minimum to simplify spares

**Restrictions and Suggestions:**

0) The 2 data fibres from one B-Layer module must be an adjacent even-odd pair

1) A consistent mapping of data to streams should be maintained

2) It is suggested that the first (Even) fibre carries bits 0 and 2, while the second (Odd) fibre carries bits 1 and 3

3) Within these restrictions, the ROD burden should be shared reasonably evenly between the loaded formatters.

4) A scheme that would suit is: (module 6 is not always present)

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Layers B Layer
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**Layers B Layer**

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Layers B Layer

PROVISIONAL
Layer 1 Notes:

Pixel Requirements (Provisional):

0) 1 Clock and Control fibre per module
1) 1 Data fibre per module: even and odd data bits are time multiplexed onto the one fibre, giving a data rate of 80 MBit/s per Pixel module.
2) 13 modules per BOC/ROD
3) all fibres connect as 8-way ribbons: 2 Clock and Control ribbons, and 2 Data ribbons

BOC and ROD Loading:

0) BOC needs only 2 Opto-TX cards loaded in locations OTX0 and OTX1 (?? or 0 & 2 ??)
2) BOC has only 2 Opto-RX cards loaded in locations ORX0 and ORX4
3) BOC needs only PHOS4 Data Delay chips for BOC streams [11:0] and [59:48] (i.e. 6 PHOS4s)
4) BOC has only 2 RX-PLDs loaded, RX-PLD0 and RX-PLD2
5) ROD has only 4 Formatters loaded in locations [0,1,4,5]
6) BOC loading may be more than the minimum to simplify spares

Restrictions and Suggestions:

0) A consistent mapping of data to streams should be maintained
1) Within these restrictions, the ROD burden should be shared reasonably evenly between the loaded formatters.
2) A scheme that would suit is:

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PROVISIONAL
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Layers Layer 1

PROVISIONAL
### Layer 2 and Disk Notes:

**Pixel Requirements (Provisional):**

1. **Layer 2 and Disks**

   **0) 1 Clock and Control fibre per module**
   
   1) 1 Data fibre per module with a data rate of 40 MBit/s
   
   2) 26 modules per BOC/ROD

   **3) all fibres connect as 8-way ribbons: 4 Clock and Control ribbons, and 4 Data ribbons**

**BOC and ROD Loading:**

**0) BOC needs all 4 Opto-TX cards loaded**

1) ROD needs only serve Clock and Control streams [9:2], [21:14], [33:26], and [45:38]

2) BOC has only 4 Opto-RX cards loaded in locations ORX0, ORX1, ORX4, and ORX5

3) BOC needs only PHOS4 Data Delay chips for BOC streams [23:0] and [71:48] (i.e. 12 PHOS4s)

4) BOC has only 2 RX-PLDs loaded, RX-PLD0 and RX-PLD2

5) ROD has only 4 Formatters loaded in locations [0,1,4,5]

6) All Pixel BOCs may be loaded to this level to simplify spares

### Restrictions and Suggestions:

0) A consistent mapping of data to streams should be maintained

1) **Within these restrictions, the ROD burden should be shared reasonably evenly between**
   
   **the loaded formatters.**

2) **A scheme that would suit is:**

| Module | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
|--------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Ribbon | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 3 | 3 | 3 | 3 |
| Fibre  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 0 | 1 | 1 | 2 | 3 | 4 | 5 | 6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 0 | 1 | 2 |
| BOC #: | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| ROD #: | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Format | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Layers Layer 2 and Disks

PROVISIONAL
Layers Layer 2 and Disks

PROVISIONAL
### Layer 2 and Disk Mapping (first half)

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**Layers Layer 2 and Disks**

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Layer 2 and Disk Mapping (2nd half)

Layers Layer 2 and Disks

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