

## BOC Series Set-Up Bus Top Level Address Map (Atlas User View)

Mnemonic	SetUpBus Add (hex)	Function	Mnemonic	SetUpBus Add (hex)	Function
TXDACS:	200		CREGS:	400	
	1E0			3C0	BOC Control
	1C0			3A0	
	140	TX Laser Current DACs		380	Monitoring
	180			360	
	160			340	RX Threshold DACs
	140			320	
	120			300	
	100			2E0	Delay Strobes
	0F0	BPM12_3 Lasers[47:36]		2C0	
0E0		2A0			
0D0		280			
0C0	BPM12_2 Lasers[35:24]	260	Clock Phases		
0B0		240			
0A0	BPM12_1 Lasers[23:12]	220	Delays		
090		200			
080	BPM12_0 Lasers[11:0]				
070					
060					
050					
040					
030					
020					
010					
BPMS:	000		RXDELAYS:	200	

**BPM12 Registers (BPM12 Registers are Read-Write)**

Address Offset (Hex)	Rel. Last#	Function	Bits	Reset Value (Dec)
+37	None	Test Circuit Control Word 1 Bit 6 (0x40) Inhibits Internal Clock	?	?
+36				
+35				
+34				
+33	None	Test Circuit Control Word 0 Bit 5 (0x20) Inhibits RAND & TRIG O/Ps	?	?
+32				
+31				
+30				
+2F	11	Fine Delay	6:0	0
+2E	11	Coarse Delay	4:0	0
+2D	11	Mark-Space	4:0	11 (~50%)
+2C	11	Stream Inhibit	0:0	0 (=Enabled)
+2B	10	Fine Delay	6:0	0
+2A	10	Coarse Delay	4:0	0
+29	10	Mark-Space	4:0	11 (~50%)
+28	10	Stream Inhibit	0:0	0 (=Enabled)
+27	9	Fine Delay	6:0	0
+26	9	Coarse Delay	4:0	0
+25	9	Mark-Space	4:0	11 (~50%)
+24	9	Stream Inhibit	0:0	0 (=Enabled)
+23	8	Fine Delay	6:0	0
+22	8	Coarse Delay	4:0	0
+21	8	Mark-Space	4:0	11 (~50%)
+20	8	Stream Inhibit	0:0	0 (=Enabled)
+1F	7	Fine Delay	6:0	0
+1E	7	Coarse Delay	4:0	0
+1D	7	Mark-Space	4:0	11 (~50%)
+1C	7	Stream Inhibit	0:0	0 (=Enabled)
+1B	6	Fine Delay	6:0	0
+1A	6	Coarse Delay	4:0	0
+19	6	Mark-Space	4:0	11 (~50%)
+18	6	Stream Inhibit	0:0	0 (=Enabled)
+17	5	Fine Delay	6:0	0
+16	5	Coarse Delay	4:0	0
+15	5	Mark-Space	4:0	11 (~50%)
+14	5	Stream Inhibit	0:0	0 (=Enabled)
+13	4	Fine Delay	6:0	0
+12	4	Coarse Delay	4:0	0
+11	4	Mark-Space	4:0	11 (~50%)
+10	4	Stream Inhibit	0:0	0 (=Enabled)
+0F	3	Fine Delay	6:0	0
+0E	3	Coarse Delay	4:0	0
+0D	3	Mark-Space	4:0	11 (~50%)
+0C	3	Stream Inhibit	0:0	0 (=Enabled)
+0B	2	Fine Delay	6:0	0
+0A	2	Coarse Delay	4:0	0
+09	2	Mark-Space	4:0	11 (~50%)
+08	2	Stream Inhibit	0:0	0 (=Enabled)
+07	1	Fine Delay	6:0	0
+06	1	Coarse Delay	4:0	0
+05	1	Mark-Space	4:0	11 (~50%)
+04	1	Stream Inhibit	0:0	0 (=Enabled)
+03	0	Fine Delay	6:0	0
+02	0	Coarse Delay	4:0	0
+01	0	Mark-Space	4:0	11 (~50%)
+00	0	Stream Inhibit	0:0	0 (=Enabled)

Laser Current DACs ( see note below )					
Setup BUS ADDRESS	Laser Number	Technical Detail			
		TX MDAC #	MD_SEL	PAL	MD_SADD
1AF	47	TXMD7	0x17	TX_MDPAL	2
1AE	46				3
1AD	45				4
1AC	44				5
1AB	43				6
1AA	42				7
1A9	41				TXMD6
1A8	40	3			
1A7	39	4			
1A6	38	5			
1A5	37	6			
1A4	36	7			
1A3	35	TXMD5	0x15		2
1A2	34				3
1A1	33				4
1A0	32				5
19F	31				6
19E	30	7			
19D	29	TXMD4	0x14		2
19C	28				3
19B	27				4
19A	26				5
199	25				6
198	24				7
197	23	TXMD3	0x13		2
196	22				3
195	21				4
194	20				5
193	19			6	
192	18			7	
191	17			TXMD2	0x12
190	16	3			
18F	15	4			
18E	14	5			
18D	13	6			
18C	12	7			
18B	11	TXMD1	0x11	2	
18A	10			3	
189	9			4	
188	8			5	
187	7			6	
186	6			7	
185	5	TXMD0	0x10	2	
184	4			3	
183	3			4	
182	2			5	
181	1			6	
180	0			7	

**Note:** TX Laser Current DACs have a threshold:  
0mA up to around 150, then linear to around 18mA at 255

RX Delays and Clock Phases ( 0-24 in 1ns steps )					
SetUp BUS ADDRESS	Function	Technical Detail			
		Delay Chip #	A[5:2]	S[2:0]	I2C-Bus
23F	DataDelay 63	PHOS4_15	F	3	I <sup>2</sup> C-Bus0
23E	DataDelay 62			2	
23D	DataDelay 61			1	
23C	DataDelay 60			0	
23B	DataDelay 59	PHOS4_14	E	3	
23A	DataDelay 58			2	
239	DataDelay 57			1	
238	DataDelay 56			0	
237	DataDelay 55	PHOS4_13	D	3	
236	DataDelay 54			2	
235	DataDelay 53			1	
234	DataDelay 52			0	
233	DataDelay 51	PHOS4_12	C	3	
232	DataDelay 50			2	
231	DataDelay 49			1	
230	DataDelay 48			0	
22F	DataDelay 47	PHOS4_11	B	3	
22E	DataDelay 46			2	
22D	DataDelay 45			1	
22C	DataDelay 44			0	
22B	DataDelay 43	PHOS4_10	A	3	
22A	DataDelay 42			2	
229	DataDelay 41			1	
228	DataDelay 40			0	
227	DataDelay 39	PHOS4_9	9	3	
226	DataDelay 38			2	
225	DataDelay 37			1	
224	DataDelay 36			0	
223	DataDelay 35	PHOS4_8	8	3	
222	DataDelay 34			2	
221	DataDelay 33			1	
220	DataDelay 32			0	
21F	DataDelay 31	PHOS4_7	7	3	
21E	DataDelay 30			2	
21D	DataDelay 29			1	
21C	DataDelay 28			0	
21B	DataDelay 27	PHOS4_6	6	3	
21A	DataDelay 26			2	
219	DataDelay 25			1	
218	DataDelay 24			0	
217	DataDelay 23	PHOS4_5	5	3	
216	DataDelay 22			2	
215	DataDelay 21			1	
214	DataDelay 20			0	
213	DataDelay 19	PHOS4_4	4	3	
212	DataDelay 18			2	
211	DataDelay 17			1	
210	DataDelay 16			0	
20F	DataDelay 15	PHOS4_3	3	3	
20E	DataDelay 14			2	
20D	DataDelay 13			1	
20C	DataDelay 12			0	
20B	DataDelay 11	PHOS4_2	2	3	
20A	DataDelay 10			2	
209	DataDelay 9			1	
208	DataDelay 8			0	
207	DataDelay 7	PHOS4_1	1	3	
206	DataDelay 6			2	
205	DataDelay 5			1	
204	DataDelay 4			0	
203	DataDelay 3	PHOS4_0	0	3	
202	DataDelay 2			2	
201	DataDelay 1			1	
200	DataDelay 0			0	

Note 1 : The 2 VernierClock\_StepPhases add to give a range of 0-50ns in 1ns steps

Note 2 : ROD should support access to all addresses in the range 200-267 hex

RX Delays and Clock Phases ( 0-24 in 1ns steps )						
SetUp BUS ADDRESS	Function	Technical Detail			I2C-Bus	
		Delay Chip #	A[5:2]	S[2:0]		
2E4	ClockDelay 1	PHOS4_25	9	4	I <sup>2</sup> C-Bus1	
2E0	ClockDelay 0	PHOS4_24	8	4		
2DC	StrobeDelay23	PHOS4_23	7	4		
2D8	StrobeDelay22	PHOS4_22	6	4		
2D4	StrobeDelay21	PHOS4_21	5	4		
2D0	StrobeDelay20	PHOS4_20	4	4		
2CC	StrobeDelay19	PHOS4_19	3	4		
2C8	StrobeDelay18	PHOS4_18	2	4		
2C4	StrobeDelay17	PHOS4_17	1	4		
2C0	StrobeDelay16	PHOS4_16	0	4		
2BC	StrobeDelay15	PHOS4_15	F	4		I <sup>2</sup> C-Bus0
2B8	StrobeDelay14	PHOS4_14	E	4		
2B4	StrobeDelay13	PHOS4_13	D	4		
2B0	StrobeDelay12	PHOS4_12	C	4		
2AC	StrobeDelay11	PHOS4_11	B	4		
2A8	StrobeDelay10	PHOS4_10	A	4		
2A4	StrobeDelay9	PHOS4_9	9	4		
2A0	StrobeDelay8	PHOS4_8	8	4		
29C	StrobeDelay7	PHOS4_7	7	4		
298	StrobeDelay6	PHOS4_6	6	4		
294	StrobeDelay5	PHOS4_5	5	4		
290	StrobeDelay4	PHOS4_4	4	4		
28C	StrobeDelay3	PHOS4_3	3	4		
288	StrobeDelay2	PHOS4_2	2	4		
284	StrobeDelay1	PHOS4_1	1	4		
280	StrobeDelay0	PHOS4_0	0	4		
267	Not Used			3	I <sup>2</sup> C-Bus1	
266	Not Used			2		
265	VernierClock_StepPhase1	PHOS4_25	9	1		
264	VernierClock_StepPhase0			0		
263	B-Reg Clock Phase			3		
262	Not Used			2		
261	Not Used	PHOS4_24	8	1		
260	BPM Clock Phase			0		
25F	DataDelay 95			3		
25E	DataDelay 94			2		
25D	DataDelay93	PHOS4_23	7	1		
25C	DataDelay 92			0		
25B	DataDelay 91			3		
25A	DataDelay 90			2		
259	DataDelay 89	PHOS4_22	6	1		
258	DataDelay 88			0		
257	DataDelay 87			3		
256	DataDelay 86			2		
255	DataDelay 85	PHOS4_21	5	1		
254	DataDelay 84			0		
253	DataDelay 83			3		
252	DataDelay 82			2		
251	DataDelay 81	PHOS4_20	4	1		
250	DataDelay 80			0		
24F	DataDelay 79			3		
24E	DataDelay 78			2		
24D	DataDelay 77	PHOS4_19	3	1		
24C	DataDelay 76			0		
24B	DataDelay 75			3		
24A	DataDelay 74			2		
249	DataDelay 73	PHOS4_18	2	1		
248	DataDelay 72			0		
247	DataDelay 71			3		
246	DataDelay 70			2		
245	DataDelay 69	PHOS4_17	1	1		
244	DataDelay 68			0		
243	DataDelay 67			3		
242	DataDelay 66			2		
241	DataDelay 65	PHOS4_16	0	1		
240	DataDelay 64			0		

<b>First Bank of RX Threshold DACs (0:255 for 0 to 255 <math>\mu</math>A)</b>					
SetUp BUS ADDRESS	Data Stream Number	Technical Detail			
		RX MDAC #	MD_SEL	PAL	MD_SADD
32F	47	RXMD7	0x07	RX_MDPALO	2
32E	46	RXMD6	0x06		2
32D	45	RXMD7	0x07		3
32C	44	RXMD6	0x06		3
32B	43	RXMD7	0x07		4
32A	42	RXMD6	0x06		4
329	41	RXMD7	0x07		5
328	40	RXMD6	0x06		5
327	39	RXMD7	0x07		6
326	38	RXMD6	0x06		6
325	37	RXMD7	0x07		7
324	36	RXMD6	0x06		7
323	35	RXMD5	0x05		2
322	34	RXMD4	0x04		2
321	33	RXMD5	0x05		3
320	32	RXMD4	0x04		3
31F	31	RXMD5	0x05		4
31E	30	RXMD4	0x04		4
31D	29	RXMD5	0x05		5
31C	28	RXMD4	0x04		5
31B	27	RXMD5	0x05		6
31A	26	RXMD4	0x04		6
319	25	RXMD5	0x05		7
318	24	RXMD4	0x04		7
317	23	RXMD3	0x03		2
316	22	RXMD2	0x02		2
315	21	RXMD3	0x03		3
314	20	RXMD2	0x02		3
313	19	RXMD3	0x03		4
312	18	RXMD2	0x02		4
311	17	RXMD3	0x03		5
310	16	RXMD2	0x02		5
30F	15	RXMD3	0x03	6	
30E	14	RXMD2	0x02	6	
30D	13	RXMD3	0x03	7	
30C	12	RXMD2	0x02	7	
30B	11	RXMD1	0x01	2	
30A	10	RXMD0	0x00	2	
309	9	RXMD1	0x01	3	
308	8	RXMD0	0x00	3	
307	7	RXMD1	0x01	4	
306	6	RXMD0	0x00	4	
305	5	RXMD1	0x01	5	
304	4	RXMD0	0x00	5	
303	3	RXMD1	0x01	6	
302	2	RXMD0	0x00	6	
301	1	RXMD1	0x01	7	
300	0	RXMD0	0x00	7	

<b>Second Bank of RX Threshold DACs (0:255 for 0 to 255 <math>\mu</math>A)</b>					
SetUp BUS ADDRESS	Data Stream Number	Technical Detail			
		RX MDAC #	MD_SEL	PAL	MD_SADD
35F	95	RXMD15	0x0F	RX_MDPAL1	2
35E	94	RXMD14	0x0E		2
35D	93	RXMD15	0x0F		3
35C	92	RXMD14	0x0E		3
35B	91	RXMD15	0x0F		4
35A	90	RXMD14	0x0E		4
359	89	RXMD15	0x0F		5
358	88	RXMD14	0x0E		5
357	87	RXMD15	0x0F		6
356	86	RXMD14	0x0E		6
355	85	RXMD15	0x0F		7
354	84	RXMD14	0x0E		7
353	83	RXMD13	0x0D		2
352	82	RXMD12	0x0C		2
351	81	RXMD13	0x0D		3
350	80	RXMD12	0x0C		3
34F	79	RXMD13	0x0D		4
34E	78	RXMD12	0x0C		4
34D	77	RXMD13	0x0D		5
34C	76	RXMD12	0x0C		5
34B	75	RXMD13	0x0D		6
34A	74	RXMD12	0x0C		6
349	73	RXMD13	0x0D		7
348	72	RXMD12	0x0C		7
347	71	RXMD11	0x0B		2
346	70	RXMD10	0x0A		2
345	69	RXMD11	0x0B		3
344	68	RXMD10	0x0A		3
343	67	RXMD11	0x0B		4
342	66	RXMD10	0x0A		4
341	65	RXMD11	0x0B		5
340	64	RXMD10	0x0A		5
33F	63	RXMD11	0x0B	6	
33E	62	RXMD10	0x0A	6	
33D	61	RXMD11	0x0B	7	
33C	60	RXMD10	0x0A	7	
33B	59	RXMD9	0x09	2	
33A	58	RXMD8	0x08	2	
339	57	RXMD9	0x09	3	
338	56	RXMD8	0x08	3	
337	55	RXMD9	0x09	4	
336	54	RXMD8	0x08	4	
335	53	RXMD9	0x09	5	
334	52	RXMD8	0x08	5	
333	51	RXMD9	0x09	6	
332	50	RXMD8	0x08	6	
331	49	RXMD9	0x09	7	
330	48	RXMD8	0x08	7	

Monitoring					
Addr	Read Function	Bits	Write Function	Label	Note
385	ADC Data[11:8]	[0,0,0,0,D11,D10,D9,D8]	No Action	aMON_MS DAT	[4],[5]
384	ADC Data[7:0]	[D7:D0]	No Action	aMON_LS DAT	[4],[5]
383	No Action	Don't Care	No Action	aMON_SPARE	
382	No Action	Don't Care	ADC Convert	aMON_CONV	[3]
381	No Action	Channel Number (0-11)	ADC Config	aMON_FIG	[2]
380	No Action	Don't Care	ADC SetUp	aMON_SUP	[1]

Notes:	
[1]	Write to this address to initialise the Monitor ADC chip - data is ignored.
[2]	Write Channel Number here to select which parameter will be converted (see below).
[3]	Write to this address to perform an ADC CONVERT: data ignored.
[4]	Read from these addresses to get the result of the last ADC CONVERT.
[5]	Series BOCs with HW_Rev = 0 have a 10-Bit ADC: for them, use Reading = [D9:D0,0,0]
[6] below	This is average of VPIN for streams[0:23] and VPIN for streams[24:47]: so get half expected value when one is tripped.
[7] below	This is average of VPIN for streams[48:71] and VPIN for streams[72:95]: so get half expected value when one is tripped.

Channels:					
Channel	Parameter		Formulae		Note
			BOC RevA	BOC RevB&C	
0	PIN Current	Stream[0:11]	1	4	
1	PIN Current	Stream[12:23]	1	4	
2	PIN Current	Stream[24:35]	1	4	
3	PIN Current	Stream[36:47]	1	4	
4	PIN Current	Stream[48:59]	1	4	
5	PIN Current	Stream[60:71]	1	4	
6	PIN Current	Stream[72:83]	1	4	
7	PIN Current	Stream[84:95]	1	4	
8	PIN Voltage	Stream[0:47]	2	5	[6]
9	PIN Voltage	Stream[48:95]	2	5	[7]
10	Thermistor 1		3	6	
11	Thermistor 2		3	6	

Formulae:						
RevA/ RevB	Number	Formula Form	Parameter Values		Range	Nominal
			K	M	Max	Value
RevA	1	$K + M * \text{Reading}$	41520 uA	-10.147 uA/ct	41.52 mA	
	2	$M * \text{Reading}$		2.777 mV/ct	11.36 V	8.42 V
	3	$R_{Therm} = K * ((M / \text{Reading}) - 1)$	10000 Ohm	4095		10K @ 25
RevB & RevC	4	$K + M * \text{Reading}$	-97 uA	5.958 uA/ct	24.375 mA	
	5	$M * \text{Reading}$		3.623 mV/ct	14.83 V	9.78 V
	6	$R_{Therm} = K * ((M / \text{Reading}) - 1)$	10000 Ohm	4095		10K @ 25

Getting Temperature from RTherm:					
Thermistor Used	ATC Semitec 103KT1608 to VADC with 10K to ground				
Steinhart-Hart Formula	$1/T \text{ (Kelvin)} = C0 + C1 * \ln(R_{Therm}) + C3 * (\ln(R_{Therm}))^3$				
Parameters Optimised over 20 - 100 Deg C	RevA	C0	7.4717E-04		
		C1	2.7726E-04		
		C3	6.8388E-08		
	RevB & RevC	C0	7.4717E-04		
		C1	2.7726E-04		
		C3	6.8388E-08		

BOC Controls					
Addr	Read Function	Bits	Write Function	Label	Note
3DF					
3DE					
3CD					
3DC					
3DB					
3DA					
3D9					
3D8	Serial No. (board switches)	[7:0]	No Action	MOD_SN	
3D7					
3D6					
3D5					
3D4					
3D3	Manufacturer = CB (hex)	[7:0]	No Action	MANUF	
3D2	Module Type = 46 (dec)	[7:0]	No Action	MOD_TYPE	[1]
3D1	Hardware Revision	[7:0]	No Action	HW_REV	[2]
3D0	Firmware Revision	[7:0]	No Action	FIRM_REV	
3CF					
3CE					
3CD					
3CC					
3CB					
3CA	Clock Control Bits	[4:0]	Clock Control Bits	CK_CONT	[3]
3C9	Reserved		Reserved		
3C8	Vernier Clock Fine Phase	[7:0]	Vernier Clock Fine Phase	VC_FPh	[4]
3C7					
3C6					
3C5	RX Data Mode	[2:0]	RX Data Mode	RXDMODE	[7]
3C4	BOC Status	[7:0]	No Action	BOCSTAT	[5]
3C3					
3C2					
3C1					
3C0	BOC Reset	[7:0]	BOC Reset	BOCRST	[6]

**Notes:**

- [0] ROD should support access to the whole range 3c0-3df hex - they may be used by later revisions
- [1] Module type is 46 for RevA and RevB BOCs. Prototype BOCs were type 44
- [2] Hardware Revision is 1 for RevA, and Currently 2 for RevB: this may increment
- [3] Clock Control word: [P4\_DIV4,BPMPH\_Bypass,VernierStep\_Bypass,Half\_Clock,Clock\_Invert]
- [4] Vernier Clock Fine Phase: [7:0] sets delay in 40ps steps (0-10ns)
- [5] BOCSTATUS [REM\_LAS\_EN,LOC\_LAS\_EN,ROD\_SENSE,ERR\_FLAG,VA\_OK,VB\_OK,BOC\_OK\_REG,x]
- [6] BOC\_Reset [BPMRESET,TXD\_CLR,RXD\_CLR,VPIN\_RST,BOC\_OK\_REG\_PRESET,x,x,x]
- [7] RX Modes:

Mode#	Action
0	SCT Normal (B-Reg)
1	SCT Timing (B- & V-Reg)
2	Pixel Layer 2 (40Mb/s remapped)
3	Pixel Layer 1 & B (80 Ms/s remapped)
4	"AND" reference clocks (test mode)
5	"OR" reference clocks (test mode)
6	Clock as Data (test mode)
7	Transparent



<b>Revision Record</b>		
<b>Date</b>	<b>Sheets Affected</b>	<b>Note</b>
29-Aug-03		Updated for BOC_Series - for both RevA and RevB
04-Nov-03	Monitoring, Controls	Updated
05-Dec-03	RIG2	BOC-RIG2 Address Map added
27-Feb-04	Monitoring	Modified to work with 12-Bit ADC (as well as 10-Bit ones)
13-Mar-06	BOC Controls	Added details for extra register contents

<b>Notes</b>	
<b>Sheets Affected</b>	<b>Note</b>