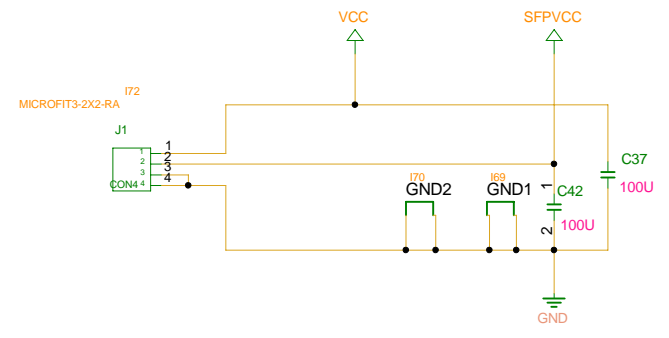
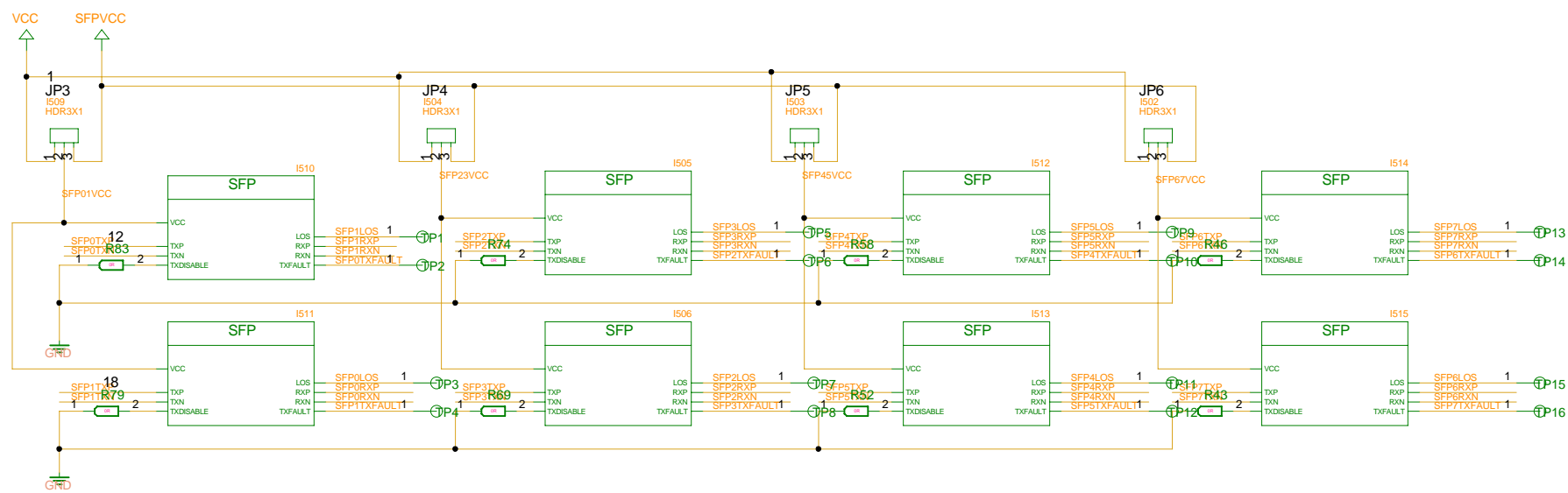
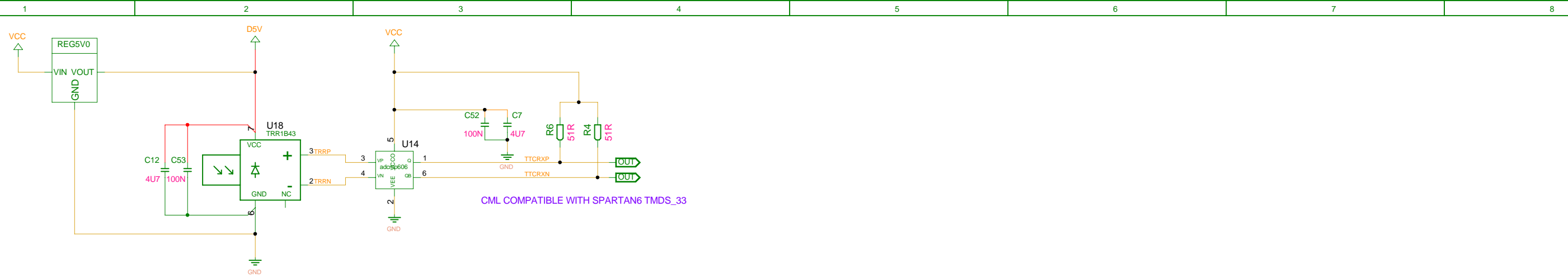
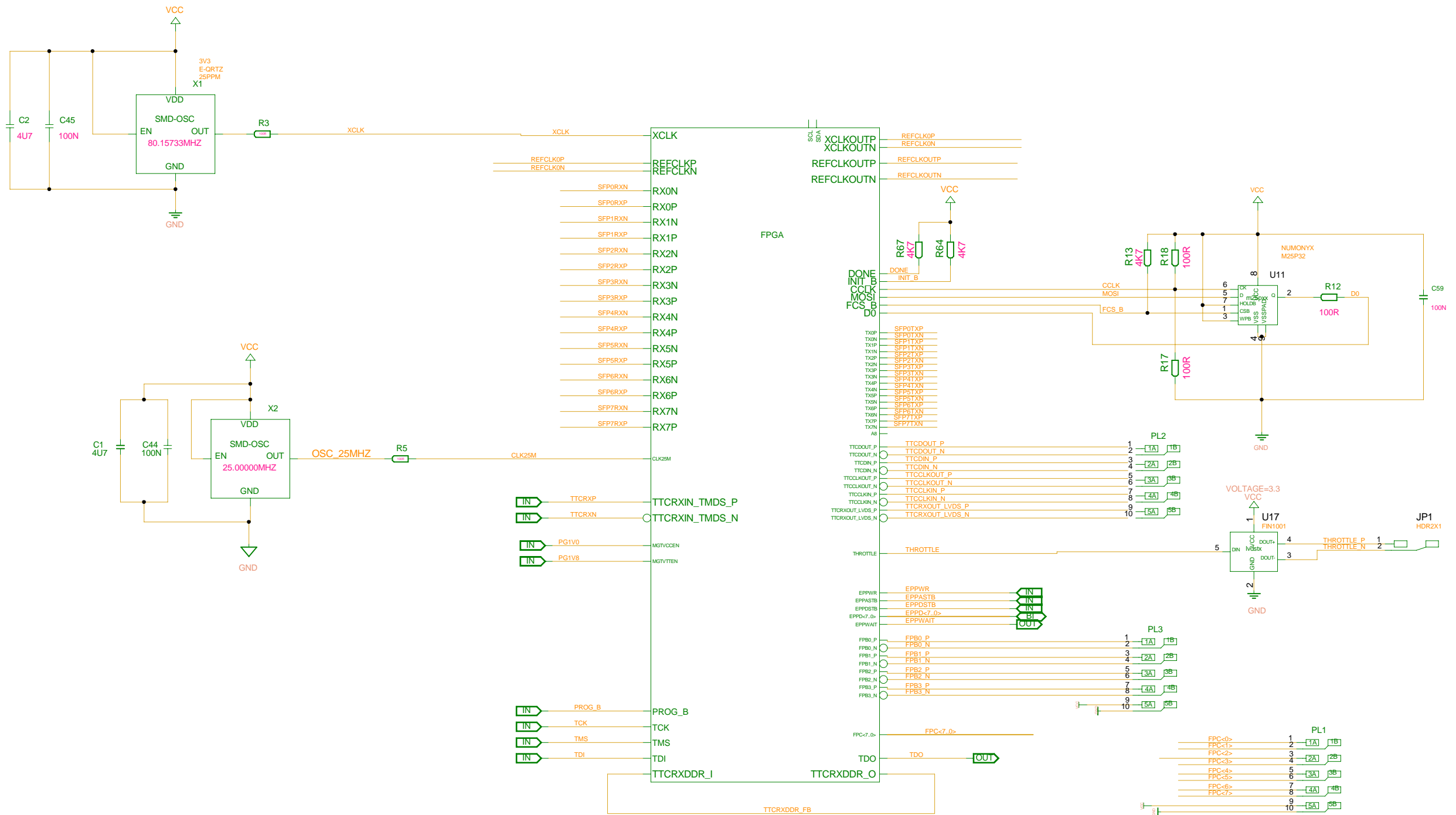


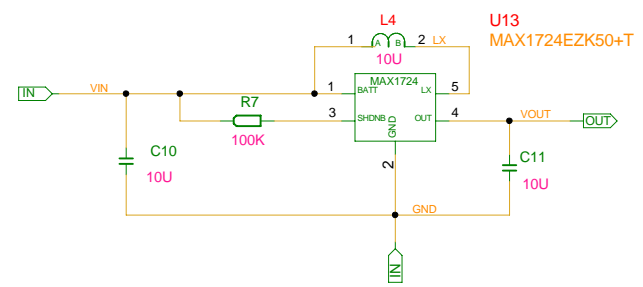
$V_{OUT} = 0.62 * (1 + R_{TOP}/R_{BOT})$

VOUT	RTOP	RBOT
1.0	191K	309K
1.2	274K	294K
1.8	301K	158K





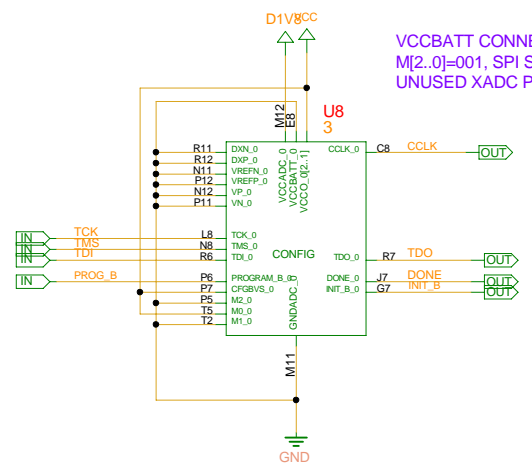




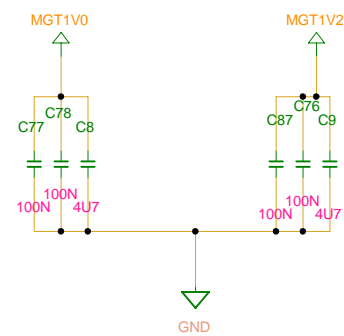
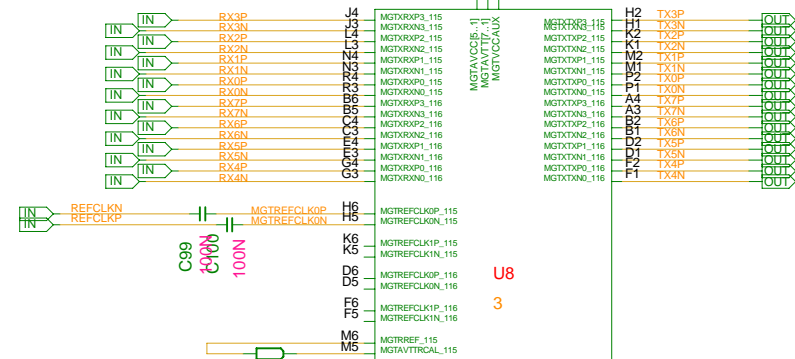
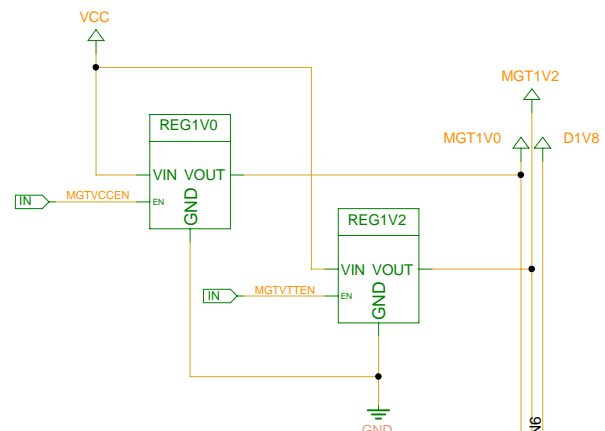
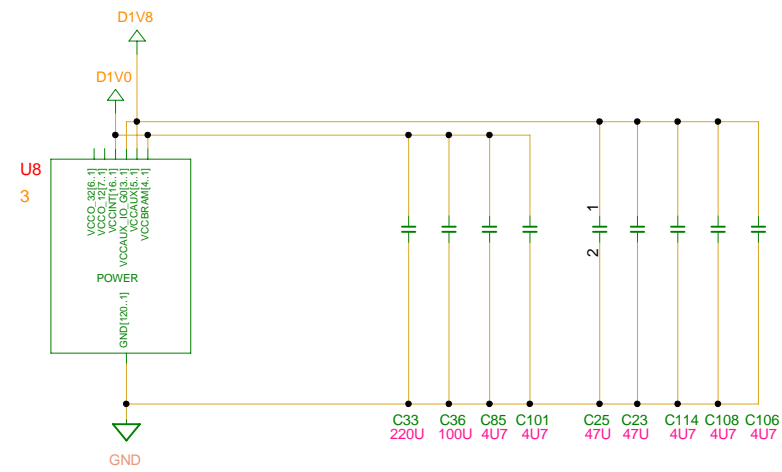
UNIVERSITY OF CAMBRIDGE HEP

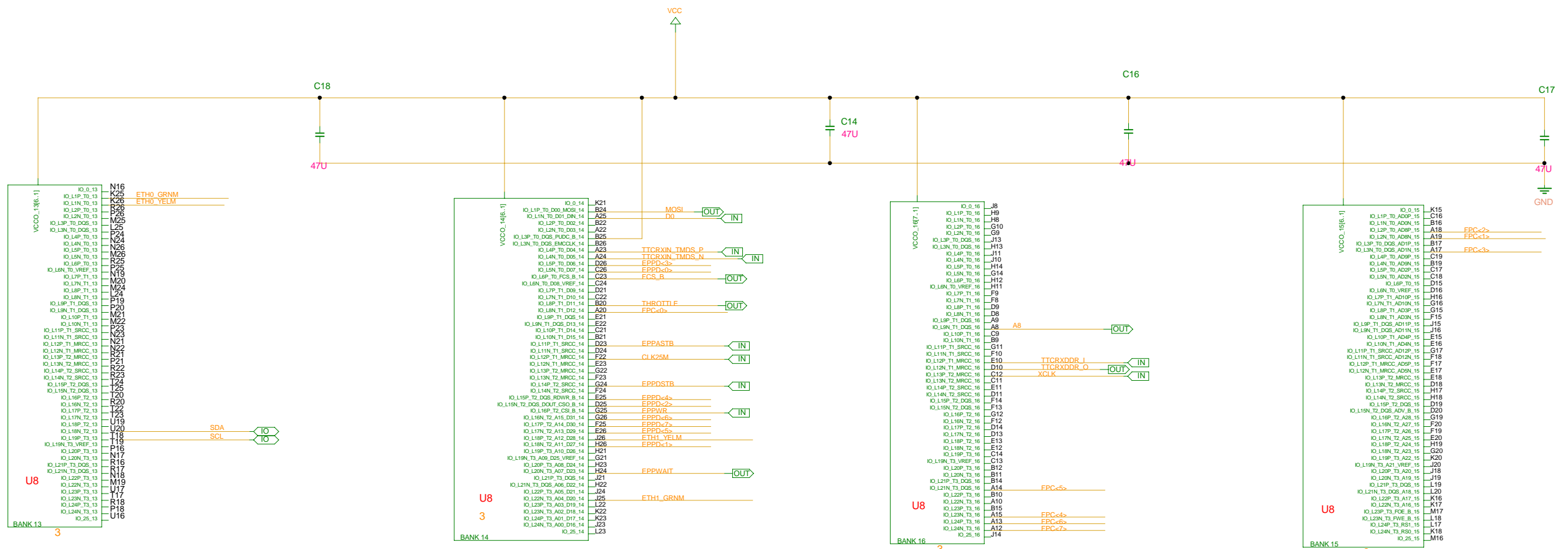
reg5v0

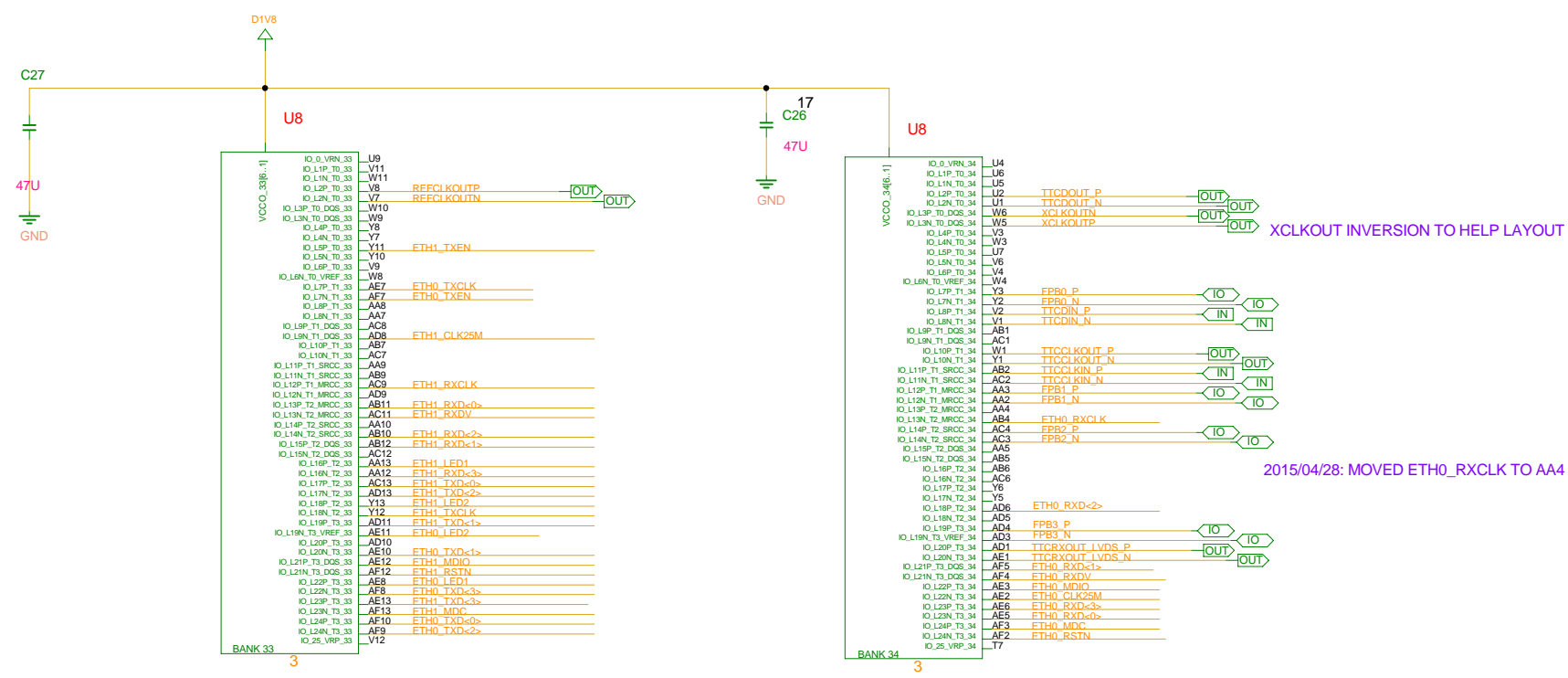
Mon Oct 03 09:46:03 2016



VCCBATT CONNECTED TO GND AS NOT USED
 M[2..0]=001, SPI SLAVE MODE
 UNUSED XADC PINS TIED ACCORDING TO RECOMMENDATIONS

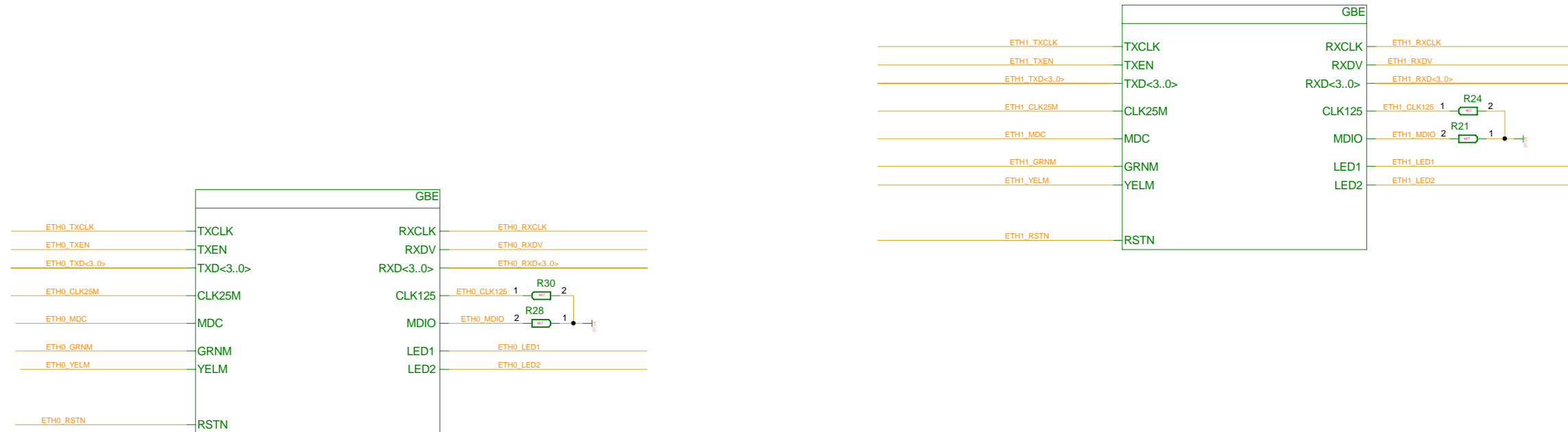


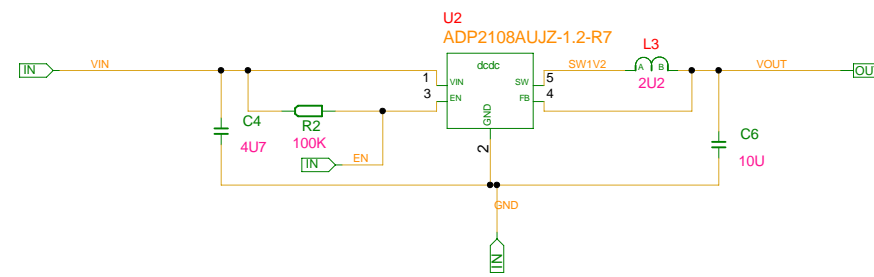


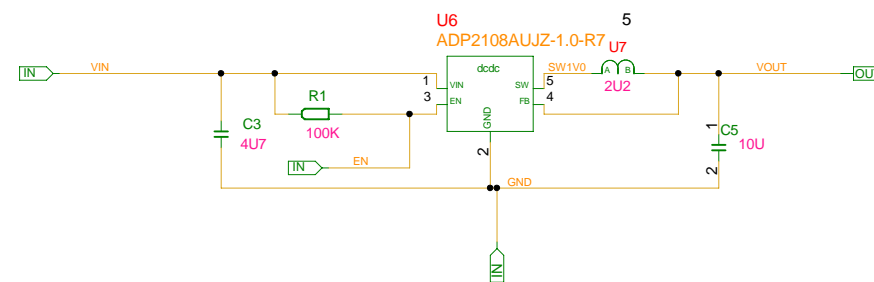


XCLKOUT INVERSION TO HELP LAYOUT

2015/04/28: MOVED ETH0_RXCLK TO AA4 (MASTER) FROM AB4 (SLAVE)

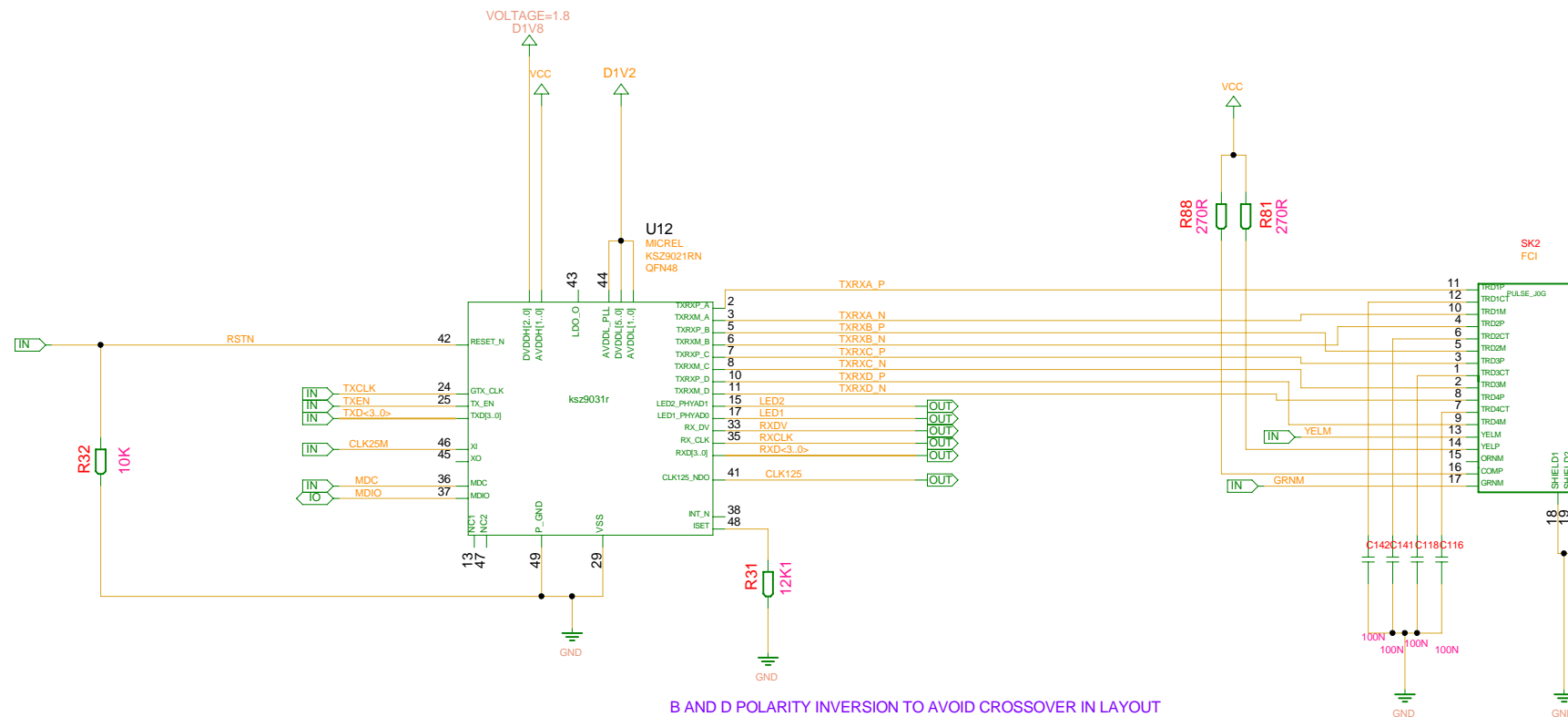




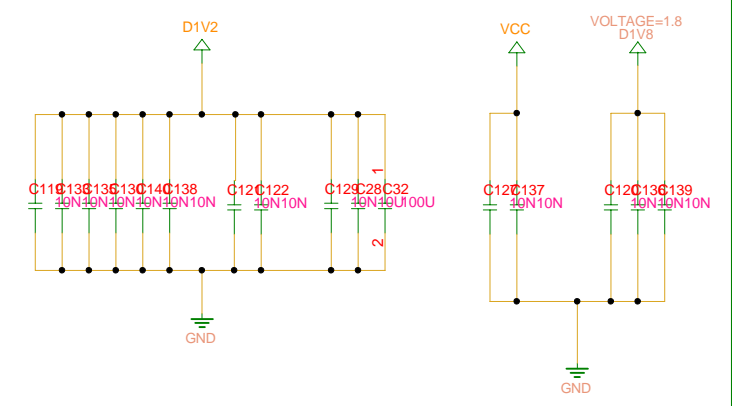


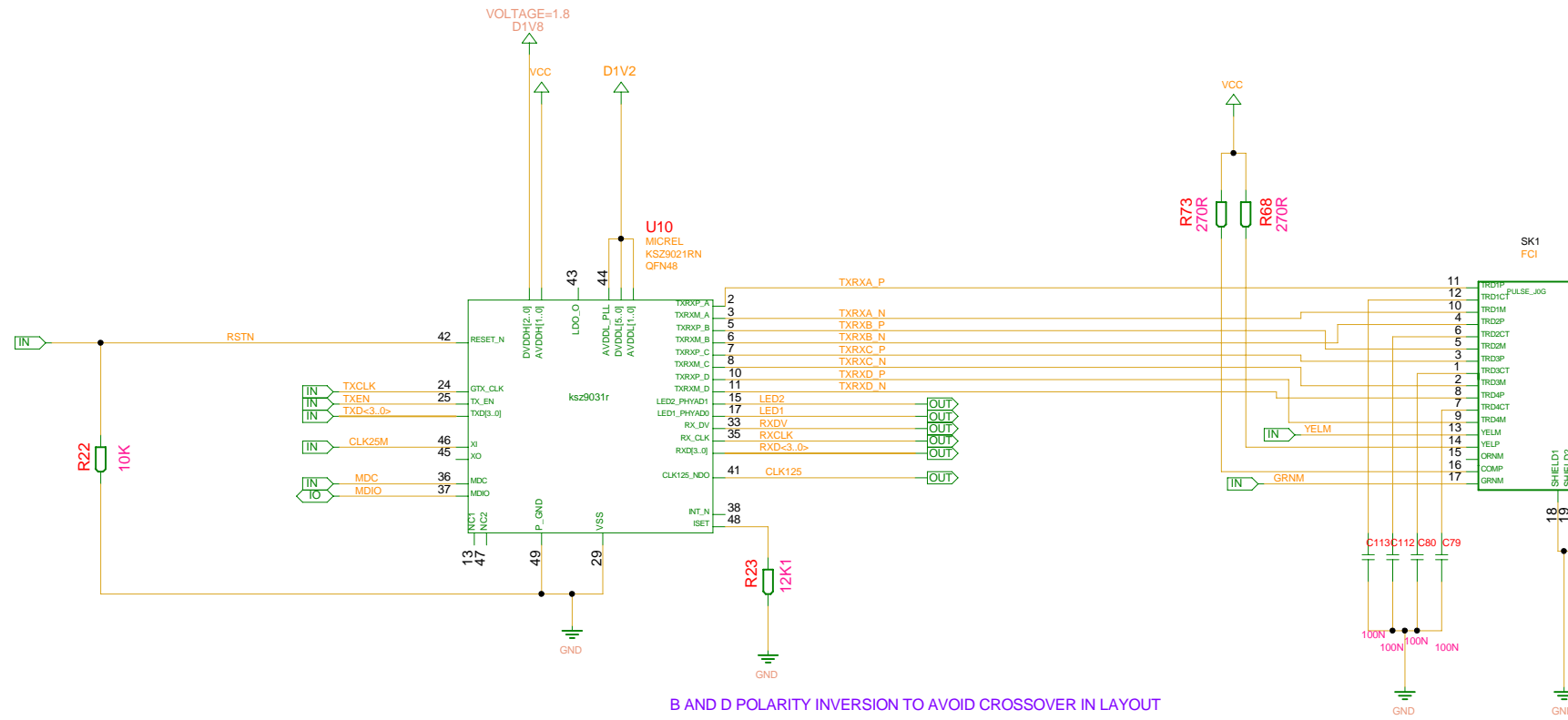
UNIVERSITY OF CAMBRIDGE HEP
reg1v0

Mon Oct 03 09:46:03 2016



B AND D POLARITY INVERSION TO AVOID CROSSOVER IN LAYOUT
 FPGA PULLUPS ON RXD<3..0> (MODE<3..0>)
 FPGA PULLDOWN ON RXCLK (PHYAD<2>)
 FPGA PULLUP ON RXDV (CLK125_NDO ENABLE)
 FPGA PULLDOWN ON CLK125_NDO (LED MODE)
 FPGA PULLDOWNS ON LED1,LED2 (PHYAD<0,1>)





B AND D POLARITY INVERSION TO AVOID CROSSOVER IN LAYOUT
 FPGA PULLUPS ON RXD<3..0> (MODE<3..0>)
 FPGA PULLDOWN ON RXCLK (PHYAD<2>)
 FPGA PULLUP ON RXDV (CLK125_NDO ENABLE)
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