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UNIVERSITY OF CAMBRIDGE HEP

mudaqv3

USB/JTAG

Wed Jul 18 15:38:55 2018

SHEET 1 OF 4

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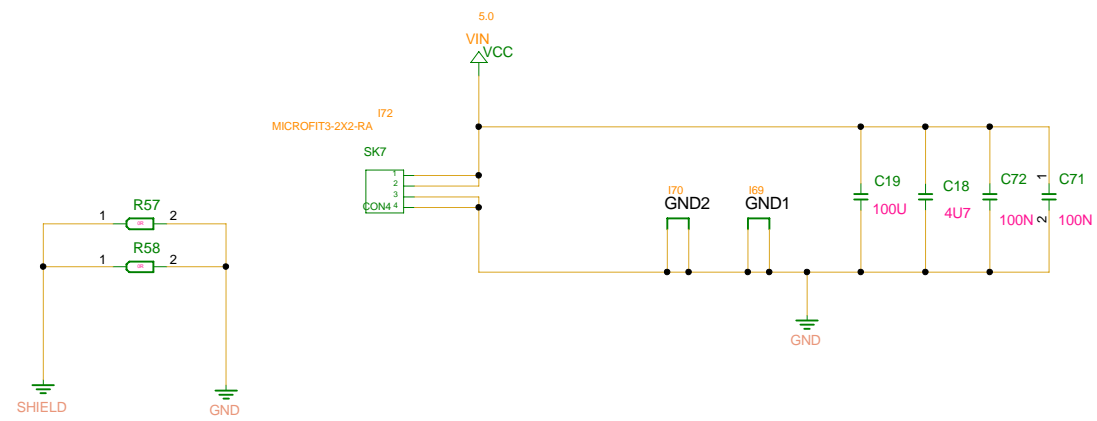
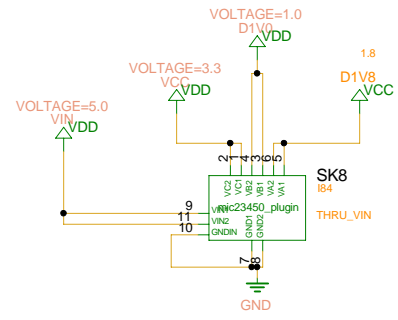
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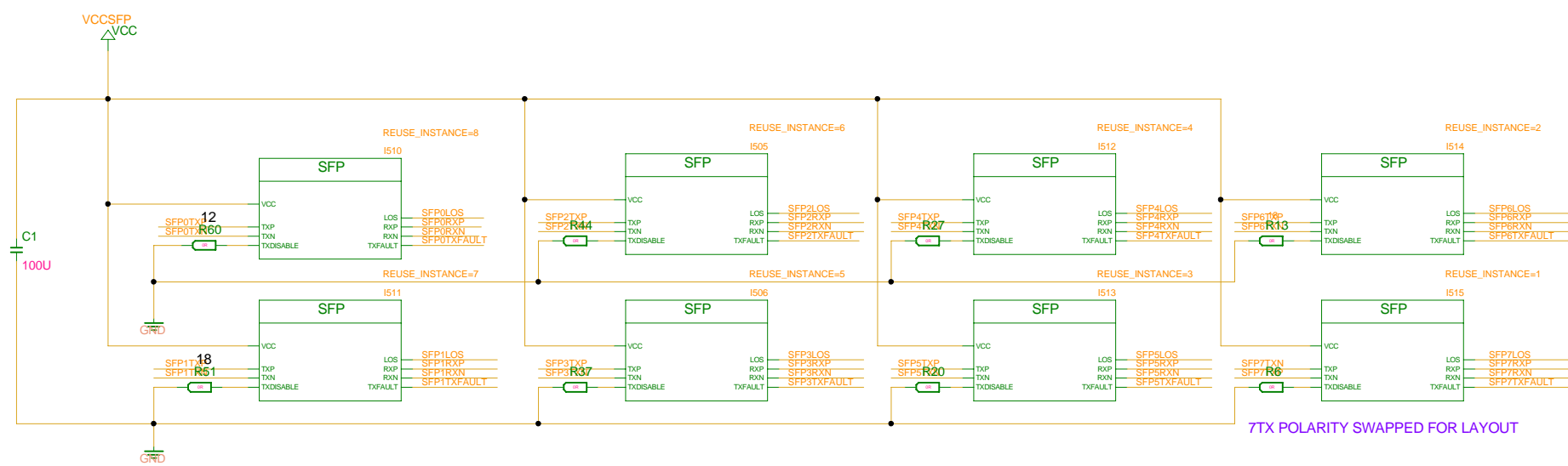
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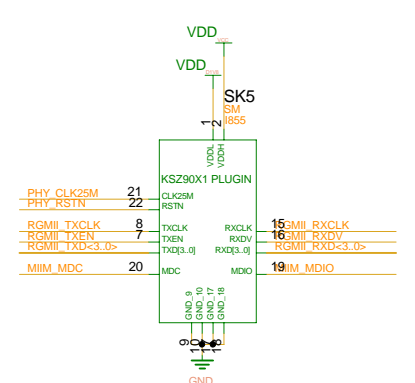
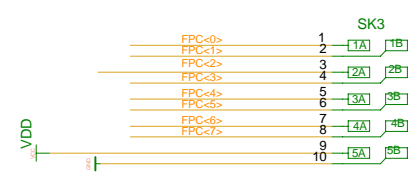
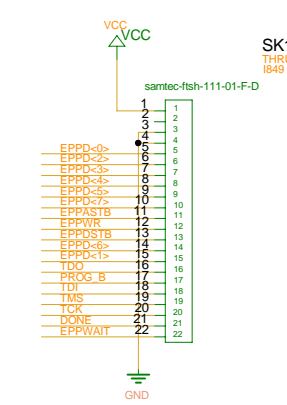
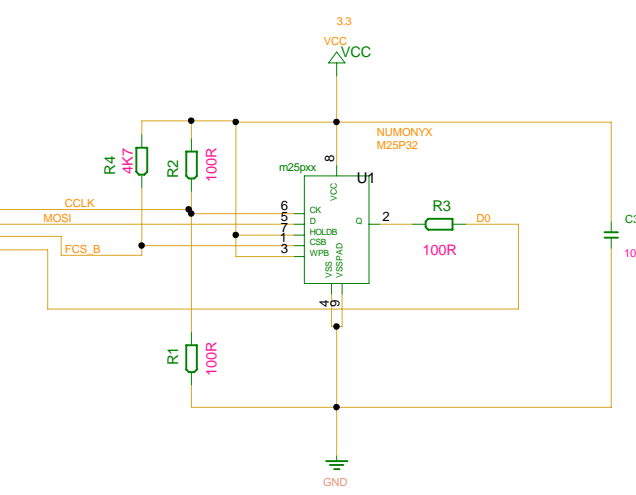
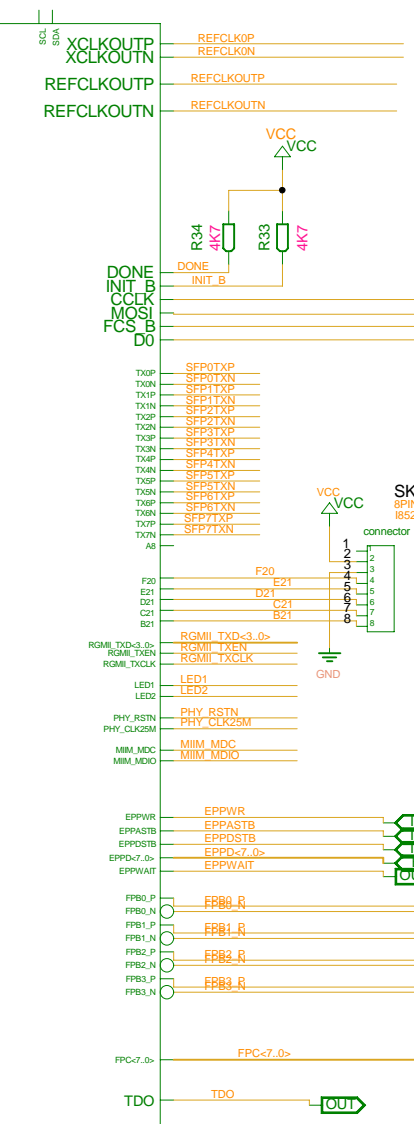
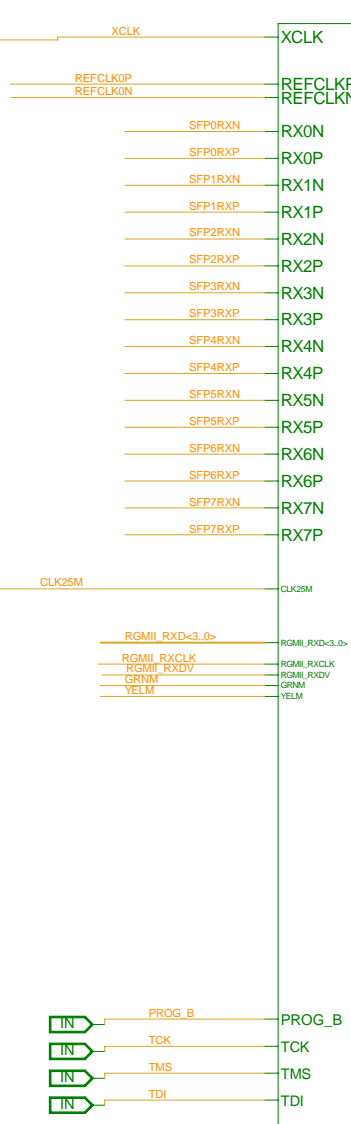
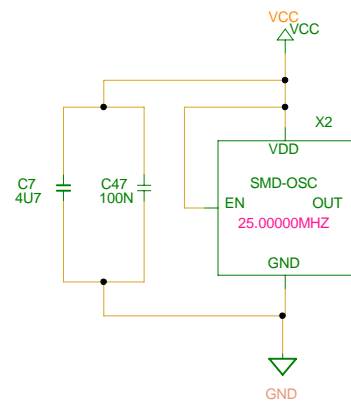
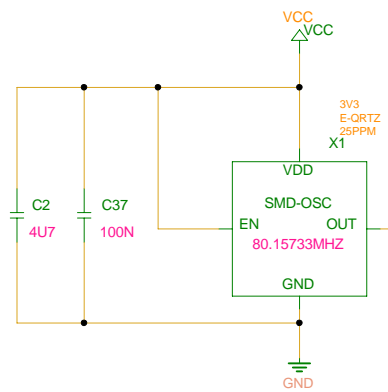
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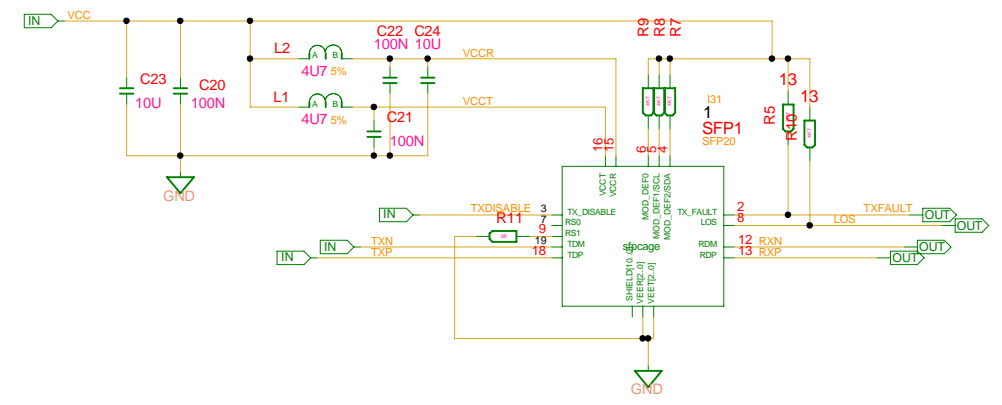
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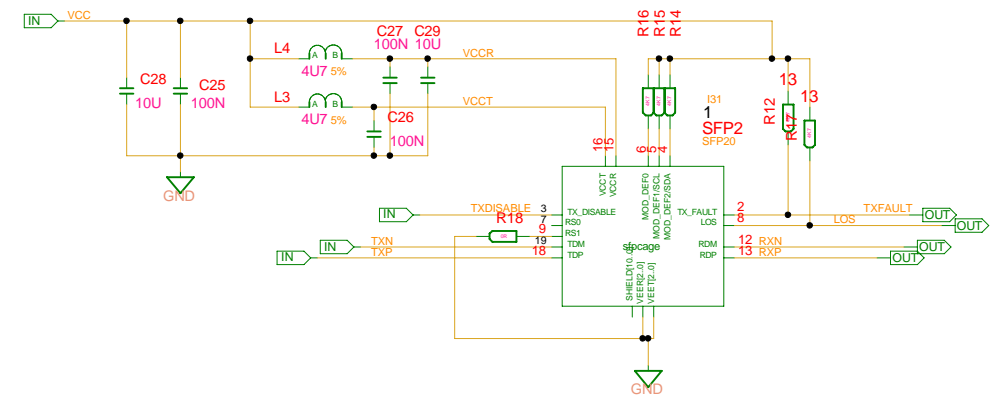


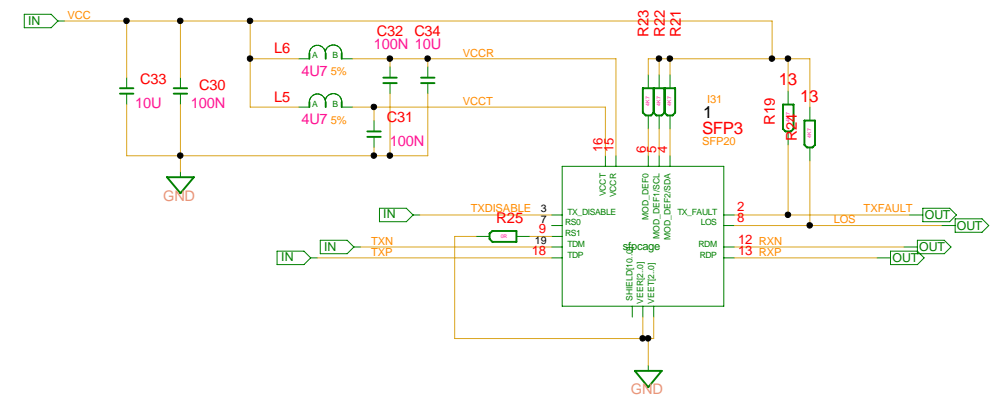


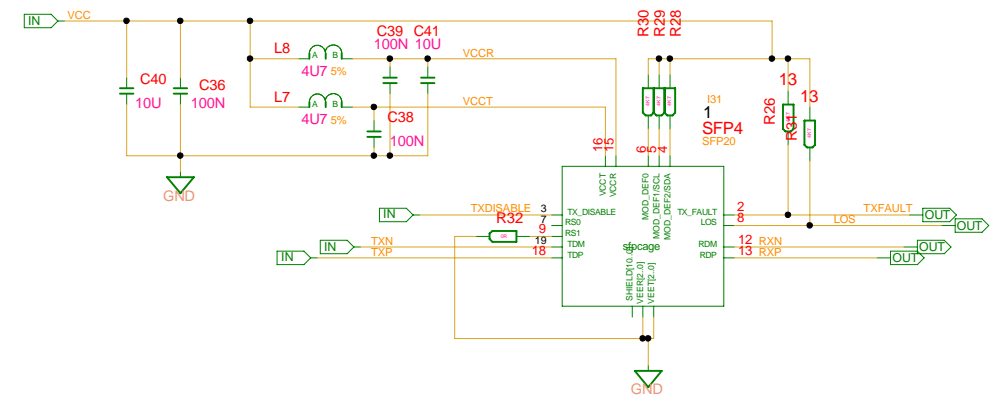


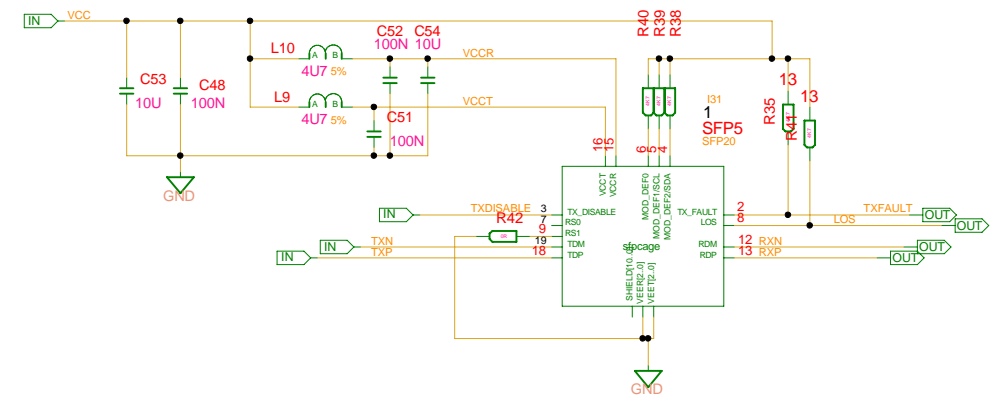
UNIVERSITY OF CAMBRIDGE HEP
 mudaqv3
 FPGA
 Fri Jul 20 16:42:35 2018







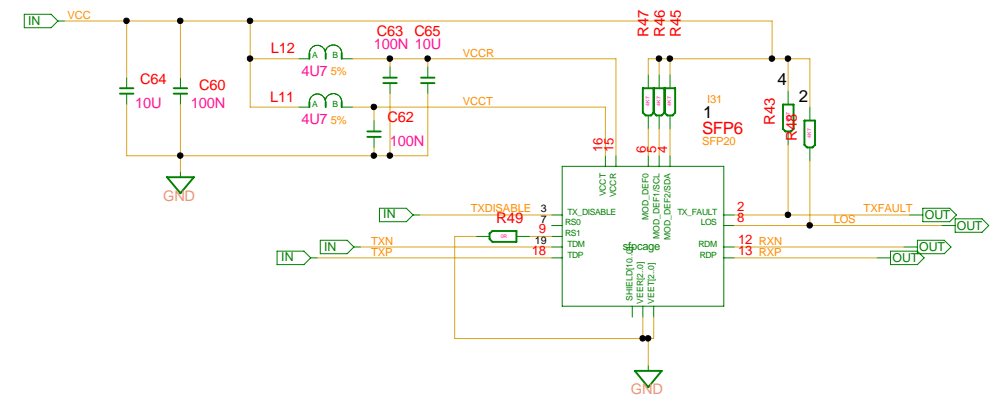


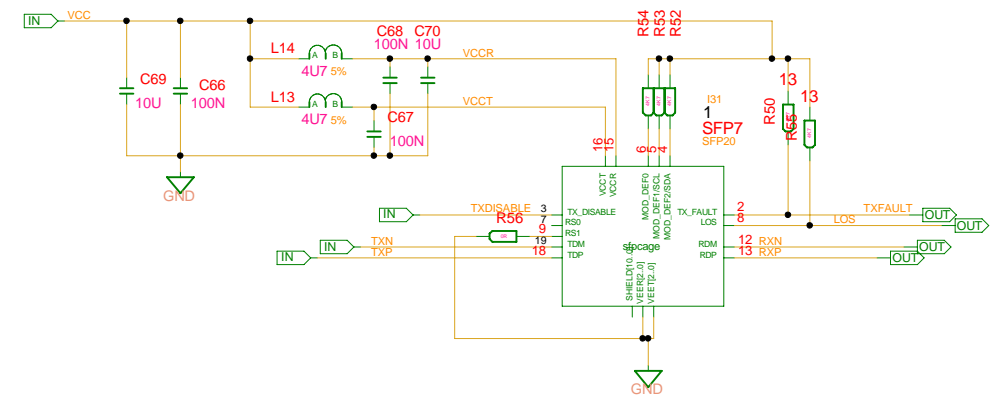


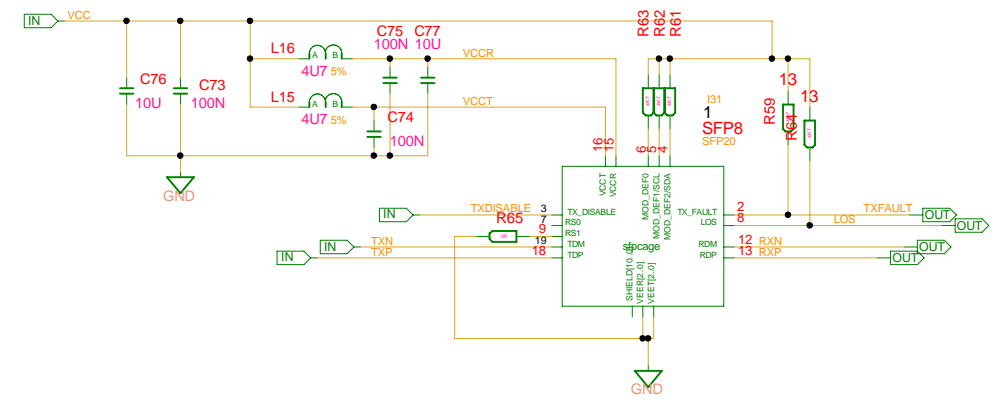
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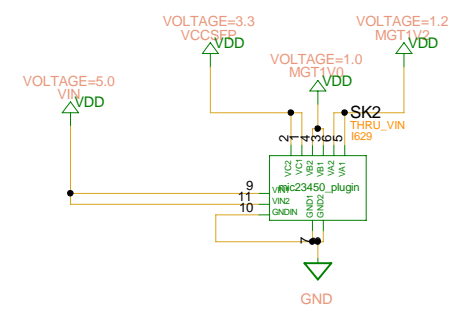
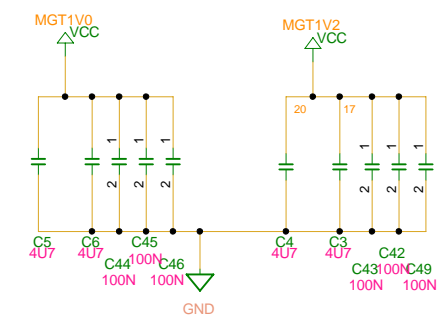
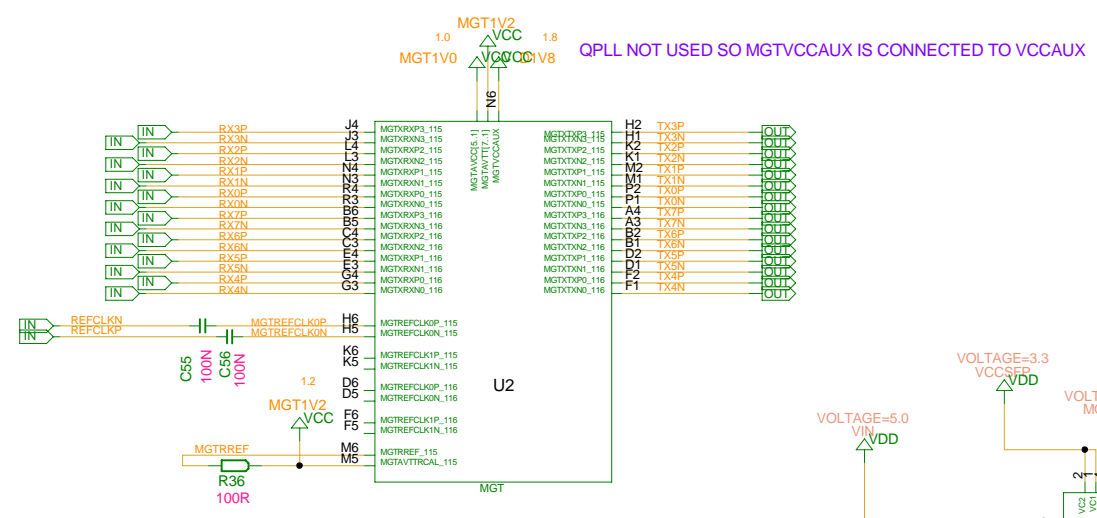
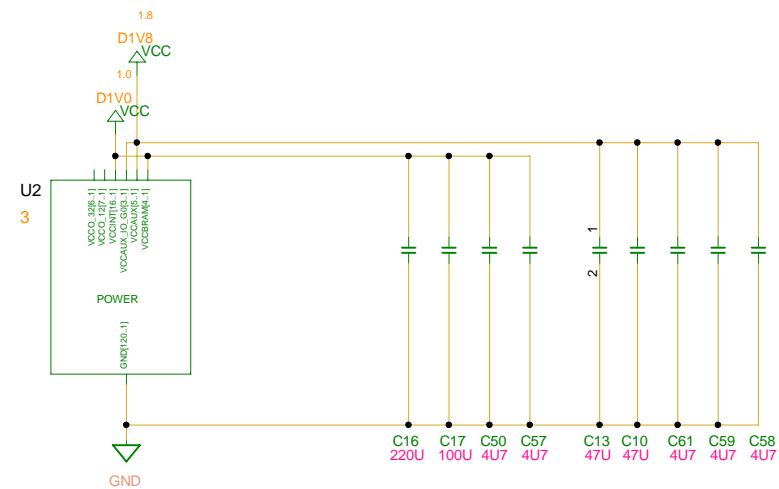
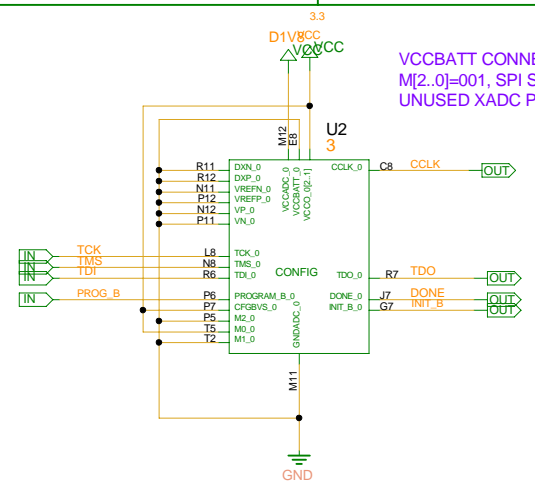
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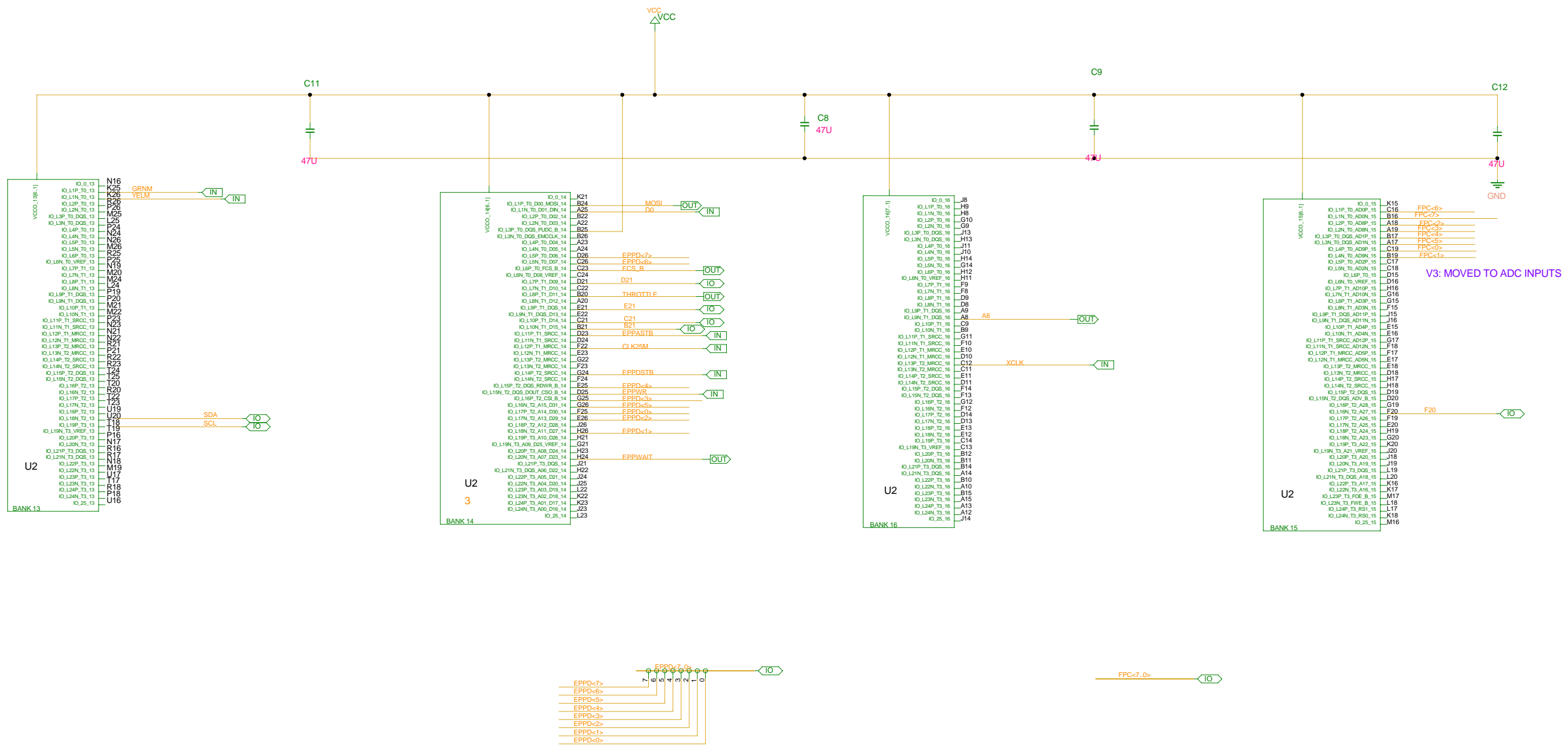
Tue Jul 17 18:13:15 2018

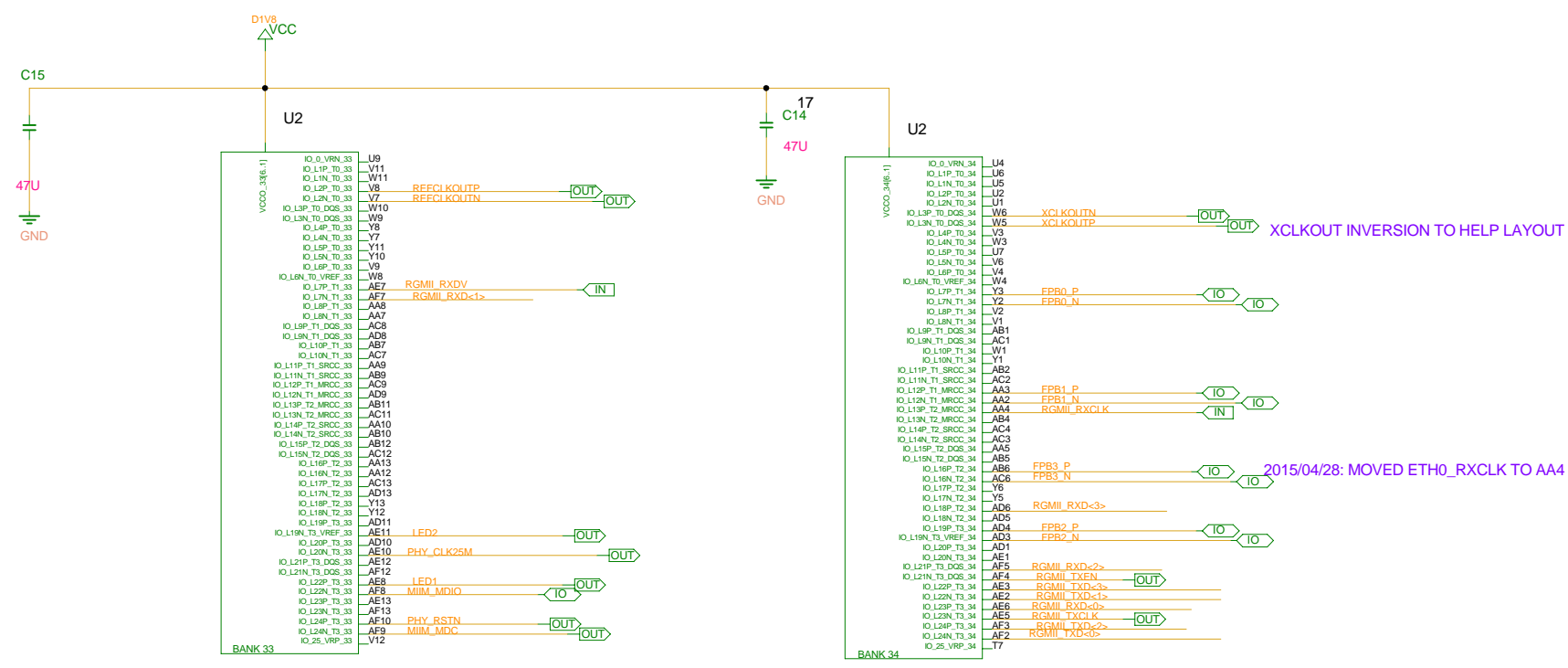












XCLKOUT INVERSION TO HELP LAYOUT

2015/04/28: MOVED ETH0_RXCLK TO AA4 (MASTER) FROM AB4 (SLAVE)

