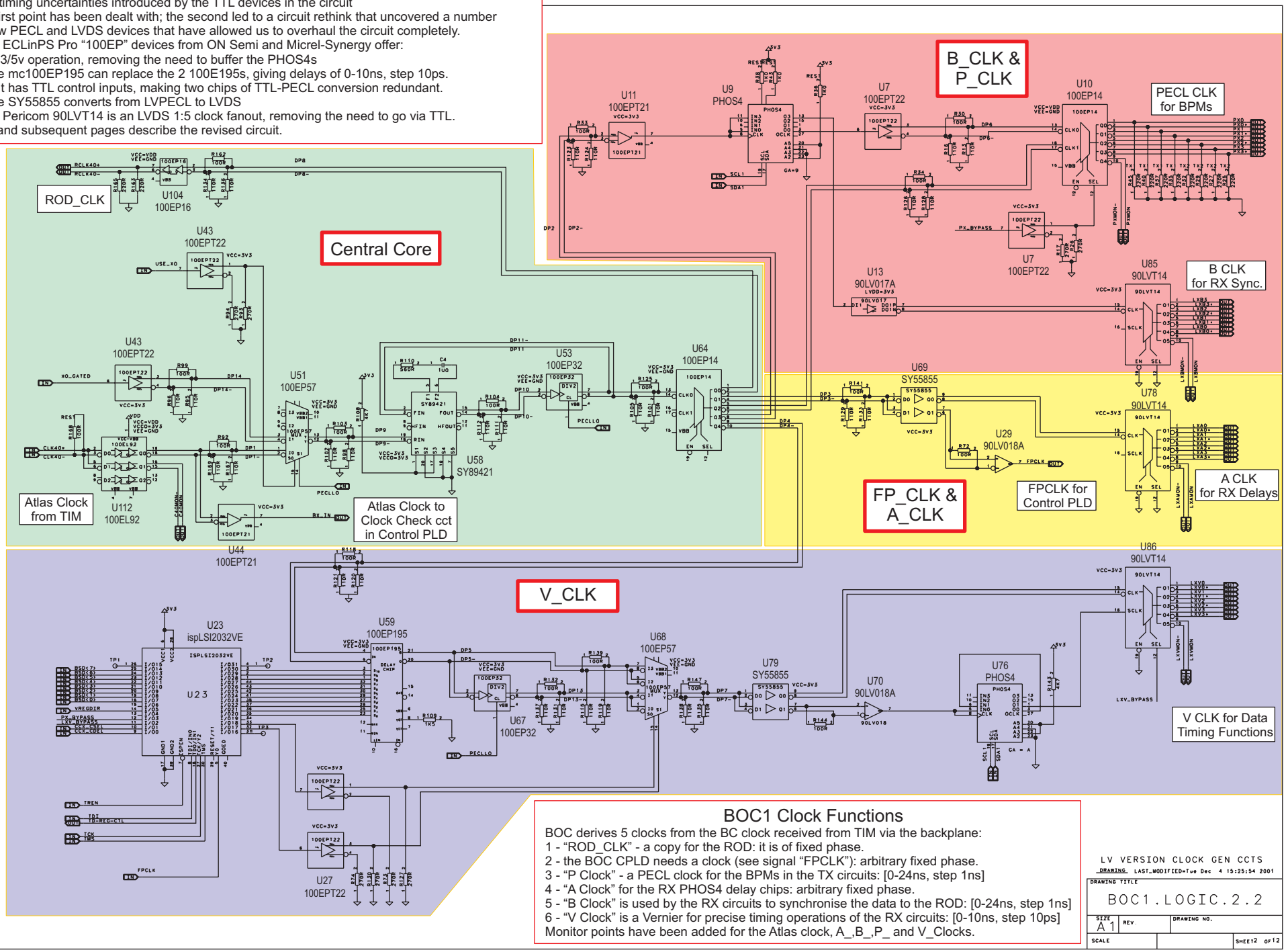
## BOC1 Revised Clock Circuits: the Why and the What

The BOC1 "Run-Thru" meeting of 15-Nov-01 concentrated on the clock circuits. Two points arose:
* the need for a dedicated signal to ROD to indicate that the fall-back clock was in use, and ...
* the timing uncertainties introduced by the TTL devices in the circuit

The first point has been dealt with; the second led to a circuit rethink that uncovered a number of new PECL and LVDS devices that have allowed us to overhaul the circuit completely.
* The ECLinPS Pro "100EP" devices from ON Semi and Micrel-Synergy offer:
  : 3v3/5v operation, removing the need to buffer the PHOS4s
  : the mc100EP195 can replace the 2 100E195s, giving delays of 0-10ns, step 10ps.
  It has TTL control inputs, making two chips of TTL-PECL conversion redundant.
  : the SY55855 converts from LVPECL to LVDS
* The Pericom 90LVT14 is an LVDS 1:5 clock fanout, removing the need to go via TTL.

This and subsequent pages describe the revised circuit.




## BOC1 Clock Functions

BOC derives 5 clocks from the BC clock received from TIM via the backplane:
1 - "ROD_CLK" - a copy for the ROD: it is of fixed phase.
2 - the BOC CPLD needs a clock (see signal "FPCLK"): arbitrary fixed phase.
3 - "P Clock" - a PECL clock for the BPMs in the TX circuits: [0-24ns, step 1ns]
4 - "A Clock" for the RX PHOS4 delay chips: arbitrary fixed phase.
5 - "B Clock" is used by the RX circuits to synchronise the data to the ROD: [0-24ns, step 1ns]
6 - "V Clock" is a Vernier for precise timing operations of the RX circuits: [0-10ns, step 10ps]

Monitor points have been added for the Atlas clock, A_,B_,P_ and V_Clocks.

LV VERSION CLOCK GEN CCTS
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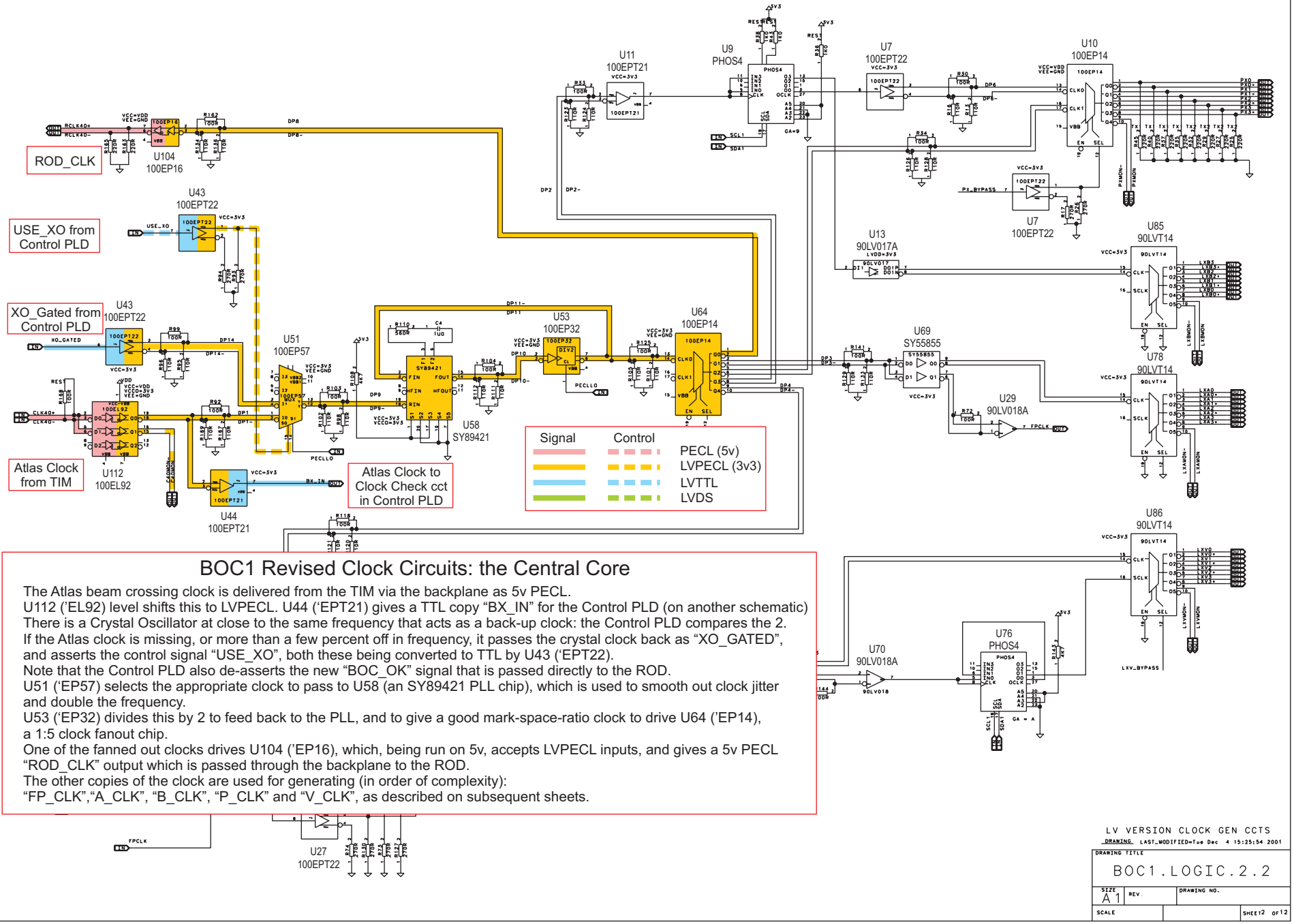


## BOC1 Revised Clock Circuits: the Central Core

The Atlas beam crossing clock is delivered from the TIM via the backplane as 5v PECL.
U112 ('EL92) level shifts this to LVPECL. U44 ('EPT21) gives a TTL copy "BX_IN" for the Control PLD (on another schematic)
There is a Crystal Oscillator at close to the same frequency that acts as a back-up clock: the Control PLD compares the 2.
If the Atlas clock is missing, or more than a few percent off in frequency, it passes the crystal clock back as "XO_GATED", and asserts the control signal "USE_XO", both these being converted to TTL by U43 ('EPT22).
Note that the Control PLD also de-asserts the new "BOC_OK" signal that is passed directly to the ROD.
U51 ('EP57) selects the appropriate clock to pass to U58 (an SY89421 PLL chip), which is used to smooth out clock jitter and double the frequency.
U53 ('EP32) divides this by 2 to feed back to the PLL, and to give a good mark-space-ratio clock to drive U64 ('EP14), a 1:5 clock fanout chip.
One of the fanned out clocks drives U104 ('EP16), which, being run on 5v, accepts LVPECL inputs, and gives a 5v PECL "ROD_CLK" output which is passed through the backplane to the ROD.
The other copies of the clock are used for generating (in order of complexity):
"FP_CLK","A_CLK", "B_CLK", "P_CLK" and "V_CLK", as described on subsequent sheets.

LV VERSION CLOCK GEN CCTS

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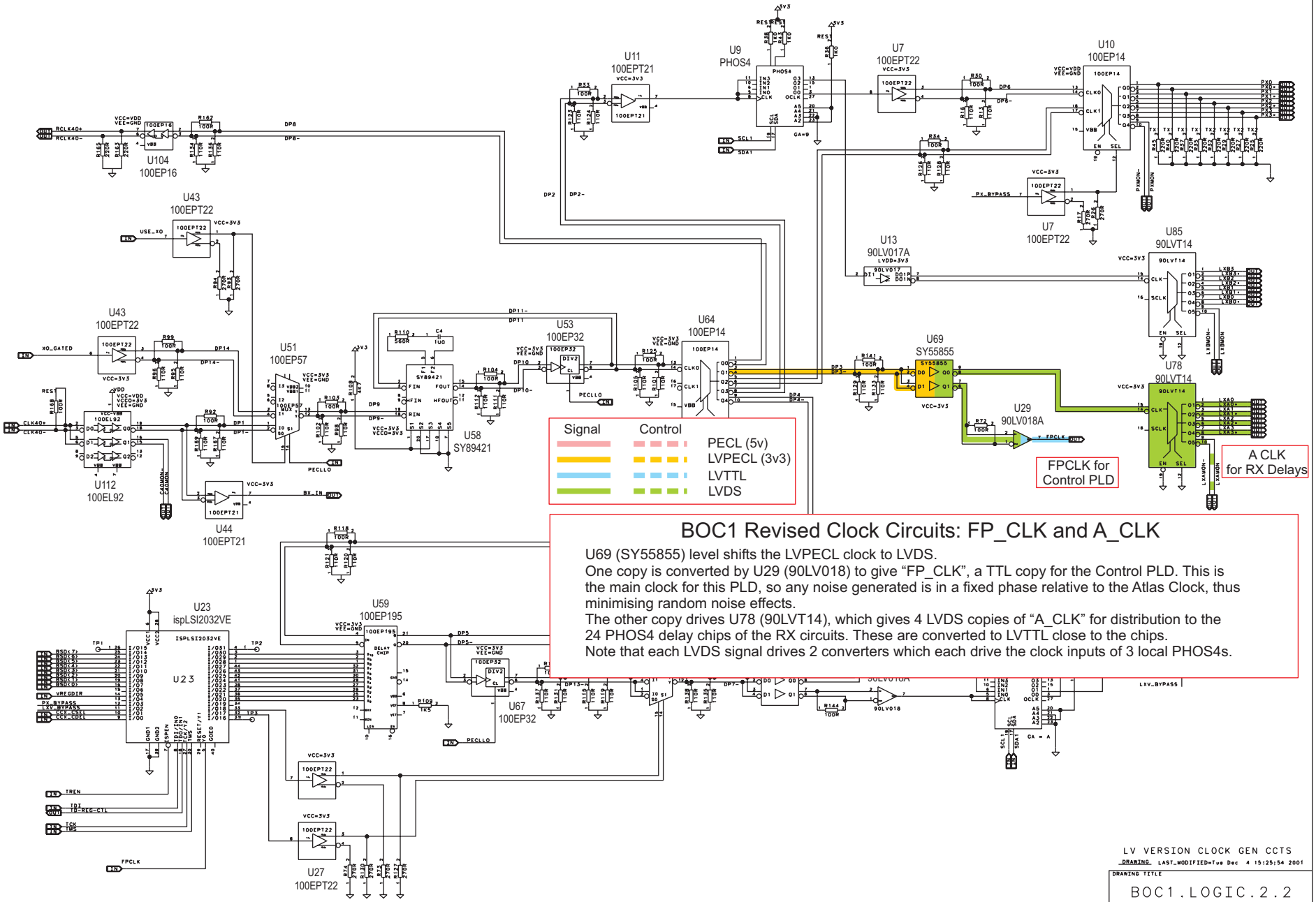
U104
100EP16
U43
100EPT22
U43
100EPT22
U43
100EPT22
U112
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U51
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100EPT21
U58
SY89421
U53
100EP32
U64
100EP14
U11
100EPT21
U9
PHOS4
U7
100EPT22
U10
100EP14
U7
100EPT22
U13
90LV017A
U85
90LVT14
U69
SY55855
U29
90LV018A
U78
90LVT14
U23
ispLSI2032VE
U59
100EP195
U67
100EP32
U27
100EPT22
Signal
Control
PECL (5v)
LVPECL (3v3)
LVTTL
LVDS
FPCLK for
Control PLD
A CLK
for RX Delays
BOC1 Revised Clock Circuits: FP_CLK and A_CLK
U69 (SY55855) level shifts the LVPECL clock to LVDS.
One copy is converted by U29 (90LV018) to give “FP_CLK”, a TTL copy for the Control PLD. This is the main clock for this PLD, so any noise generated is in a fixed phase relative to the Atlas Clock, thus minimising random noise effects.
The other copy drives U78 (90LVT14), which gives 4 LVDS copies of “A_CLK” for distribution to the 24 PHOS4 delay chips of the RX circuits. These are converted to LVTTL close to the chips.
Note that each LVDS signal drives 2 converters which each drive the clock inputs of 3 local PHOS4s.
LV VERSION CLOCK GEN CCTS
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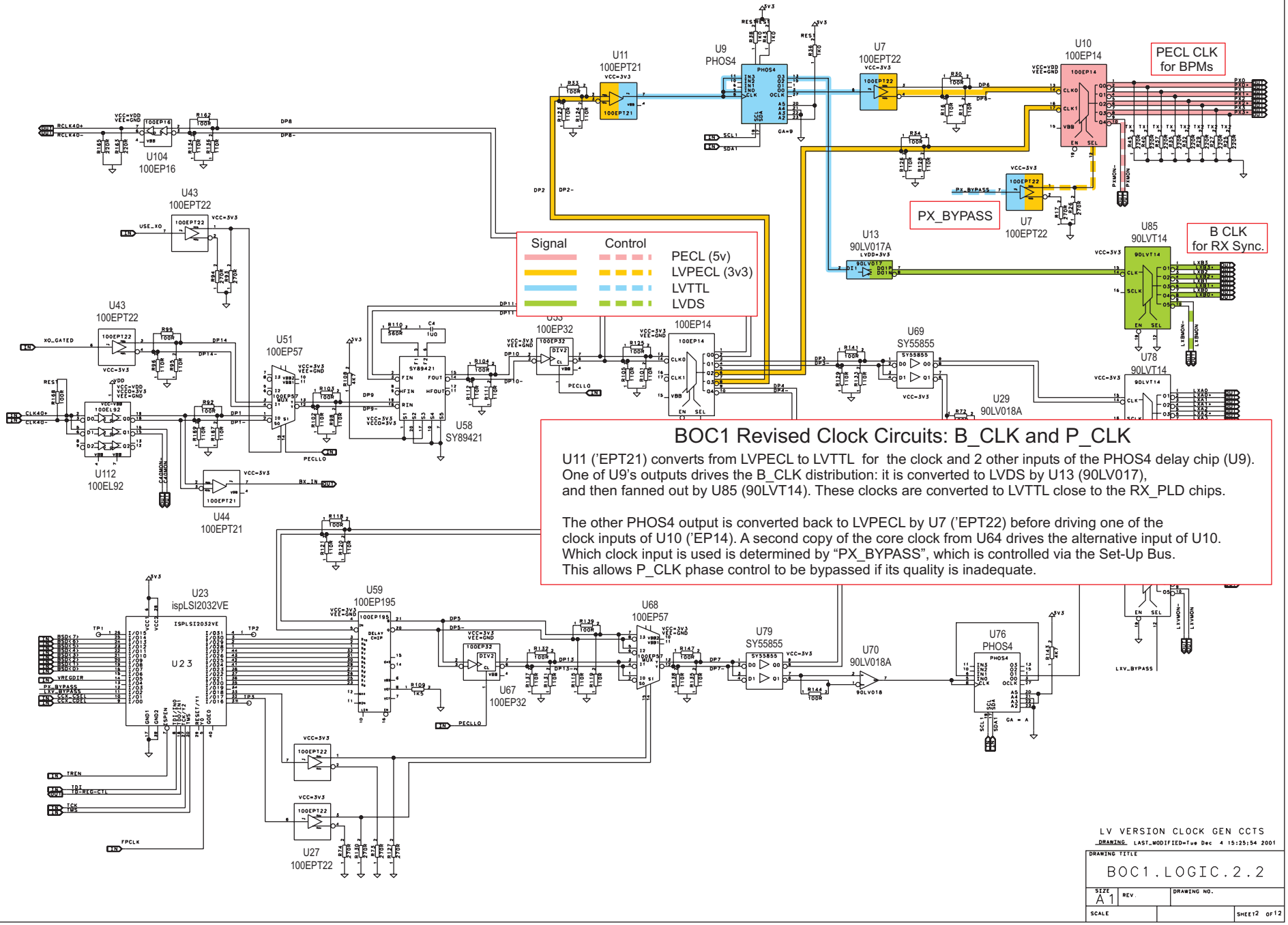
PECL CLK for BPMs
PX_BYPASS
B CLK for RX Sync.
Signal
Control
PECL (5v)
LVPECL (3v3)
LVTTL
LVDS
U11 100EPT21
U9 PHOS4
U7 100EPT22
U10 100EP14
U13 90LV017A
U85 90LVT14
U78 90LVT14
U69 SY55855
U29 90LV018A
U43 100EPT22
U51 100EP57
U33 100EP32
100EP14
U58 SY89421
U112 100EL92
U44 100EPT21
U104 100EP16
U23 ispLSI2032VE
U59 100EP195
U68 100EP57
U67 100EP32
U79 SY55855
U70 90LV018A
U76 PHOS4
U27 100EPT22
BOC1 Revised Clock Circuits: B_CLK and P_CLK
U11 ('EPT21) converts from LVPECL to LVTTL for the clock and 2 other inputs of the PHOS4 delay chip (U9).
One of U9's outputs drives the B_CLK distribution: it is converted to LVDS by U13 (90LV017),
and then fanned out by U85 (90LVT14). These clocks are converted to LVTTL close to the RX_PLD chips.
The other PHOS4 output is converted back to LVPECL by U7 ('EPT22) before driving one of the
clock inputs of U10 ('EP14). A second copy of the core clock from U64 drives the alternative input of U10.
Which clock input is used is determined by "PX_BYPASS", which is controlled via the Set-Up Bus.
This allows P_CLK phase control to be bypassed if its quality is inadequate.
LV VERSION CLOCK GEN CCTS
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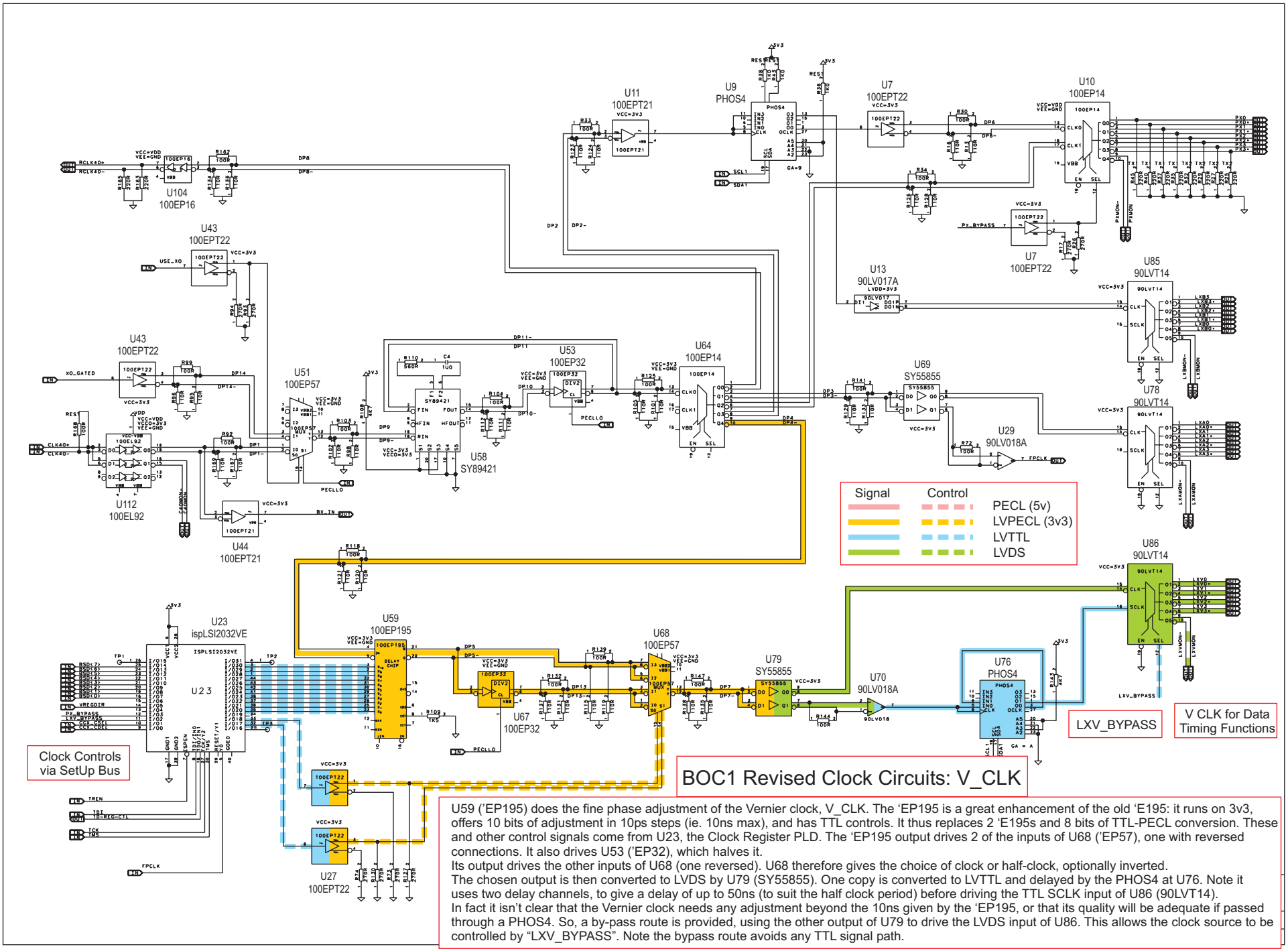


# BOC1 Revised Clock Circuits: V_CLK

U59 ('EP195) does the fine phase adjustment of the Vernier clock, V_CLK. The 'EP195 is a great enhancement of the old 'E195: it runs on 3v3, offers 10 bits of adjustment in 10ps steps (ie. 10ns max), and has TTL controls. It thus replaces 2 'E195s and 8 bits of TTL-PECL conversion. These and other control signals come from U23, the Clock Register PLD. The 'EP195 output drives 2 of the inputs of U68 ('EP57), one with reversed connections. It also drives U53 ('EP32), which halves it.

Its output drives the other inputs of U68 (one reversed). U68 therefore gives the choice of clock or half-clock, optionally inverted.

The chosen output is then converted to LVDS by U79 (SY55855). One copy is converted to LVTTL and delayed by the PHOS4 at U76. Note it uses two delay channels, to give a delay of up to 50ns (to suit the half clock period) before driving the TTL SCLK input of U86 (90LVT14).

In fact it isn't clear that the Vernier clock needs any adjustment beyond the 10ns given by the 'EP195, or that its quality will be adequate if passed through a PHOS4. So, a by-pass route is provided, using the other output of U79 to drive the LVDS input of U86. This allows the clock source to be controlled by "LXV_BYPASS". Note the bypass route avoids any TTL signal path.