BOC Series Set-Up Bus

Top Level Address Map (Engineering View)

Mnemonic	VME Add	SetUpBus Add (hex)	Function
	400	200	
	3C0	1E0	
	380	1C0	
	340	1A0	TX Laser Current DACs
TXDACS:	300	180	
	2C0	160	
	280	140	
	240	120	
	200	100	
	1E0	0F0	BPM12_3 Lasers[47:36]
	1C0	0E0	
	1A0	0D0	
	180	0C0	
	160	0B0	BPM12_2 Lasers[35:24]
	140	0A0	
	120	090	
	100	080	
	0E0	070	BPM12_1 Lasers[23:12]
	0C0	060	
	0A0	050	
	080	040	
	060	030	BPM12_0 Lasers[11:0]
	040	020	
	020	010	
BPMS:	000	000	

Mnemonic	VME Add	SetUpBus Add (hex)	Function
	800	400	
	7C0	3E0	
CREGS:	780	3C0	BOC Control
	740	3A0	
	700	380	Monitoring
	6C0	360	
	680	340	RX Threshold DACs
	640	320	
RXDACS:	600	300	
	5C0	2E0	Delay Strobes
	580	2C0	
	540	2A0	
	500	280	
CLK_PHASES:	4C0	260	Clock Phases
	480	240	Delays
	440	220	
RXDELAYS:	400	200	

BPM12 Registers (BPM12 Registers are Read-Write)

VME Add Offset	Address Offset (Hex)	Rel. Las#	Function	Bits	Reset Value (Dec)
+6E	+37	None	Test Circuit Control Word 1 Bit 6 (0x40) Inhibits Internal Clock	?	?
+6C	+36				
+6A	+35				
+68	+34				
+66	+33	None	Test Circuit Control Word 0 Bit 5 (0x20) Inhibits RAND & TRIG O/Ps	?	?
+64	+32				
+62	+31				
+60	+30				
+5E	+2F	11	Fine Delay	6:0	0
+5C	+2E	11	Coarse Delay	4:0	0
+5A	+2D	11	Mark-Space	4:0	11 (~50%)
+58	+2C	11	Stream Inhibit	0:0	0 (=Enabled)
+56	+2B	10	Fine Delay	6:0	0
+54	+2A	10	Coarse Delay	4:0	0
+52	+29	10	Mark-Space	4:0	11 (~50%)
+50	+28	10	Stream Inhibit	0:0	0 (=Enabled)
+4E	+27	9	Fine Delay	6:0	0
+4C	+26	9	Coarse Delay	4:0	0
+4A	+25	9	Mark-Space	4:0	11 (~50%)
+48	+24	9	Stream Inhibit	0:0	0 (=Enabled)
+46	+23	8	Fine Delay	6:0	0
+44	+22	8	Coarse Delay	4:0	0
+42	+21	8	Mark-Space	4:0	11 (~50%)
+40	+20	8	Stream Inhibit	0:0	0 (=Enabled)
+3E	+1F	7	Fine Delay	6:0	0
+3C	+1E	7	Coarse Delay	4:0	0
+3A	+1D	7	Mark-Space	4:0	11 (~50%)
+38	+1C	7	Stream Inhibit	0:0	0 (=Enabled)
+36	+1B	6	Fine Delay	6:0	0
+34	+1A	6	Coarse Delay	4:0	0
+32	+19	6	Mark-Space	4:0	11 (~50%)
+30	+18	6	Stream Inhibit	0:0	0 (=Enabled)
+2E	+17	5	Fine Delay	6:0	0
+2C	+16	5	Coarse Delay	4:0	0
+2A	+15	5	Mark-Space	4:0	11 (~50%)
+28	+14	5	Stream Inhibit	0:0	0 (=Enabled)
+26	+13	4	Fine Delay	6:0	0
+24	+12	4	Coarse Delay	4:0	0
+22	+11	4	Mark-Space	4:0	11 (~50%)
+20	+10	4	Stream Inhibit	0:0	0 (=Enabled)
+1E	+0F	3	Fine Delay	6:0	0
+1C	+0E	3	Coarse Delay	4:0	0
+1A	+0D	3	Mark-Space	4:0	11 (~50%)
+18	+0C	3	Stream Inhibit	0:0	0 (=Enabled)
+16	+0B	2	Fine Delay	6:0	0
+14	+0A	2	Coarse Delay	4:0	0
+12	+09	2	Mark-Space	4:0	11 (~50%)
+10	+08	2	Stream Inhibit	0:0	0 (=Enabled)
+0E	+07	1	Fine Delay	6:0	0
+0C	+06	1	Coarse Delay	4:0	0
+0A	+05	1	Mark-Space	4:0	11 (~50%)
+08	+04	1	Stream Inhibit	0:0	0 (=Enabled)
+06	+03	0	Fine Delay	6:0	0
+04	+02	0	Coarse Delay	4:0	0
+02	+01	0	Mark-Space	4:0	11 (~50%)
+00	+00	0	Stream Inhibit	0:0	0 (=Enabled)

	Laser Current DACs (see note below)					
VME	SetUp BUS	Laser Number	Technical Detail			
Add	ADDRESS		TX MDAC #	MD_SEL	PAL	MD_SADD
35E	1AF	47	TXMD7	0x17	TX_MDPAL	2
35C	1AE	46				3
35A	1AD	45				4
358	1AC	44				5
356	1AB	43				6
354	1AA	42				7
352	1A9	41	TXMD6	0x16		2
350	1A8	40				3
34E	1A7	39				4
34C	1A6	38				5
34A	1A5	37				6
348	1A4	36				7
346	1A3	35	TXMD5	0x15		2
344	1A2	34				3
342	1A1	33				4
340	1A0	32				5
33E	19F	31				6
33C	19E	30				7
33A	19D	29	TXMD4	0x14		2
338	19C	28				3
336	19B	27				4
334	19A	26				5
332	199	25				6
330	198	24				7
32E	197	23	TXMD3	0x13		2
32C	196	22				3
32A	195	21				4
328	194	20				5
326	193	19				6
324	192	18				7
322	191	17	TXMD2	0x12		2
320	190	16				3
31E	18F	15				4
31C	18E	14				5
31A	18D	13				6
318	18C	12				7
316	18B	11	TXMD1	0x11		2
314	18A	10				3
312	189	9				4
310	188	8				5
30E	187	7				6
30C	186	6				7
30A	185	5	TXMD0	0x10		2
308	184	4				3
306	183	3				4
304	182	2				5
302	181	1				6
300	180	0				7

Note: TX Laser Current DACs have a threshold:
0mA up to around 150, then linear to around 18mA at 255

	RX Delays and Clock Phases (0-24 in 1ns steps)					
VME Add	SetUp BUS ADDRESS	Function	Technical Detail			
			Delay Chip #	A[5:2]	S[2:0]	I2C-Bus
47E	23F	DataDelay 63	PHOS4_15	F	3	I^{2}C-Bus0
47C	23E	DataDelay 62			2	
47A	23D	DataDelay 61			1	
478	23C	DataDelay 60			0	
476	23B	DataDelay 59	PHOS4_14	E	3	
474	23A	DataDelay 58			2	
472	239	DataDelay 57			1	
470	238	DataDelay 56			0	
46E	237	DataDelay 55	PHOS4_13	D	3	
46C	236	DataDelay 54			2	
46A	235	DataDelay 53			1	
468	234	DataDelay 52			0	
466	233	DataDelay 51	PHOS4_12	C	3	
464	232	DataDelay 50			2	
462	231	DataDelay 49			1	
460	230	DataDelay 48			0	
45E	22F	DataDelay 47	PHOS4_11	B	3	
45C	22E	DataDelay 46			2	
45A	22D	DataDelay 45			1	
458	22C	DataDelay 44			0	
456	22B	DataDelay 43	PHOS4_10	A	3	
454	22A	DataDelay 42			2	
452	229	DataDelay 41			1	
450	228	DataDelay 40			0	
44E	227	DataDelay 39	PHOS4_9	9	3	
44C	226	DataDelay 38			2	
44A	225	DataDelay 37			1	
448	224	DataDelay 36			0	
446	223	DataDelay 35	PHOS4_8	8	3	
444	222	DataDelay 34			2	
442	221	DataDelay 33			1	
440	220	DataDelay 32			0	
43E	21F	DataDelay 31	PHOS4_7	7	3	
43C	21E	DataDelay 30			2	
43A	21D	DataDelay 29			1	
438	21C	DataDelay 28			0	
436	21B	DataDelay 27	PHOS4_6	6	3	
434	21A	DataDelay 26			2	
432	219	DataDelay 25			1	
430	218	DataDelay 24			0	
42E	217	DataDelay 23	PHOS4_5	5	3	
42C	216	DataDelay 22			2	
42A	215	DataDelay 21			1	
428	214	DataDelay 20			0	
426	213	DataDelay 19	PHOS4_4	4	3	
424	212	DataDelay 18			2	
422	211	DataDelay 17			1	
420	210	DataDelay 16			0	
41E	20F	DataDelay 15	PHOS4_3	3	3	
41C	20E	DataDelay 14			2	
41A	20D	DataDelay 13			1	
418	20C	DataDelay 12			0	
416	20B	DataDelay 11	PHOS4_2	2	3	
414	20A	DataDelay 10			2	
412	209	DataDelay 9			1	
410	208	DataDelay 8			0	
40E	207	DataDelay 7	PHOS4_1	1	3	
40C	206	DataDelay 6			2	
40A	205	DataDelay5			1	
408	204	DataDelay4			0	
406	203	DataDelay3	PHOS4_0	0	3	
404	202	DataDelay2			2	
402	201	DataDelay1			1	
400	200	DataDelay0			0	

Note 1 : The 2 VernierClock_StepPhases add to give a range of 0-50ns in 1ns steps

Note 2 : ROD should support access to all addresses in the range 200-267 hex

	RX Delays and Clock Phases (0-24 in 1ns steps)					
VME Add	SetUp BUS ADDRESS	Function	Technical Detail			
			Delay Chip #	A[5:2]	S[2:0]	I2C-Bus
5C8	2E4	ClockDelay 1	PHOS4_25	9	4	I^2C-Bus1
5C0	2E0	ClockDelay 0	PHOS4_24	8	4	
5B8	2DC	StrobeDelay23	PHOS4_23	7	4	
5B0	2D8	StrobeDelay22	PHOS4_22	6	4	
5A8	2D4	StrobeDelay21	PHOS4_21	5	4	
5A0	2D0	StrobeDelay20	PHOS4_20	4	4	
598	2CC	StrobeDelay19	PHOS4_19	3	4	
590	2C8	StrobeDelay18	PHOS4_18	2	4	
588	2C4	StrobeDelay17	PHOS4_17	1	4	
580	2C0	StrobeDelay16	PHOS4_16	0	4	
578	2BC	StrobeDelay15	PHOS4_15	F	4	I^2C-Bus0
570	2B8	StrobeDelay14	PHOS4_14	E	4	
568	2B4	StrobeDelay13	PHOS4_13	D	4	
560	2B0	StrobeDelay12	PHOS4_12	C	4	
558	2AC	StrobeDelay11	PHOS4_11	B	4	
550	2A8	StrobeDelay10	PHOS4_10	A	4	
548	2A4	StrobeDelay9	PHOS4_9	9	4	
540	2A0	StrobeDelay8	PHOS4_8	8	4	
538	29C	StrobeDelay7	PHOS4_7	7	4	
530	298	StrobeDelay6	PHOS4_6	6	4	
528	294	StrobeDelay5	PHOS4_5	5	4	
520	290	StrobeDelay4	PHOS4_4	4	4	
518	28C	StrobeDelay3	PHOS4_3	3	4	
510	288	StrobeDelay2	PHOS4_2	2	4	
508	284	StrobeDelay1	PHOS4_1	1	4	
500	280	StrobeDelay0	PHOS4_0	0	4	
4CE	267	Not Used	PHOS4_25	9	3	I^2C-Bus1
4CC	266	Not Used			2	
4CA	265	VernierClock_StepPhase1			1	
4C8	264	VernierClock_StepPhase0			0	
4C6	263	B-Reg Clock Phase	PHOS4_24	8	3	
4C4	262	Not Used			2	
4C2	261	Not Used			1	
4C0	260	BPM Clock Phase			0	
4BE	25F	DataDelay 95	PHOS4_23	7	3	
4BC	25E	DataDelay 94			2	
4BA	25D	DataDelay93			1	
4B8	25C	DataDelay 92			0	
4B6	25B	DataDelay 91	PHOS4_22	6	3	
4B4	25A	DataDelay 90			2	
4B2	259	DataDelay 89			1	
4B0	258	DataDelay 88			0	
4AE	257	DataDelay 87	PHOS4_21	5	3	
4AC	256	DataDelay 86			2	
4AA	255	DataDelay 85			1	
4A8	254	DataDelay 84			0	
4A6	253	DataDelay 83	PHOS4_20	4	3	
4A4	252	DataDelay 82			2	
4A2	251	DataDelay 81			1	
4A0	250	DataDelay 80			0	
49E	24F	DataDelay 79	PHOS4_19	3	3	
49C	24E	DataDelay 78			2	
49A	24D	DataDelay 77			1	
498	24C	DataDelay 76			0	
496	24B	DataDelay 75	PHOS4_18	2	3	
494	24A	DataDelay 74			2	
492	249	DataDelay 73			1	
490	248	DataDelay 72			0	
48E	247	DataDelay 71	PHOS4_17	1	3	
48C	246	DataDelay 70			2	
48A	245	DataDelay 69			1	
488	244	DataDelay 68			0	
486	243	DataDelay 67	PHOS4_16	0	3	
484	242	DataDelay 66			2	
482	241	DataDelay 65			1	
480	240	DataDelay 64			0	

First Bank of RX Threshold DACs (0:255 for 0 to 255 uA)						
VME	SetUp BUS	Data Stream	Technical Detail			
Add	ADDRESS	Number	RX MDAC #	MD_SEL	PAL	MD_SADD
65E	32F	47	RXMD7	0x07	RX_MDPAL0	2
65C	32E	46	RXMD6	0x06		2
65A	32D	45	RXMD7	0x07		3
658	32C	44	RXMD6	0x06		3
656	32B	43	RXMD7	0x07		4
654	32A	42	RXMD6	0x06		4
652	329	41	RXMD7	0x07		5
650	328	40	RXMD6	0x06		5
64E	327	39	RXMD7	0x07		6
64C	326	38	RXMD6	0x06		6
64A	325	37	RXMD7	0x07		7
648	324	36	RXMD6	0x06		7
646	323	35	RXMD5	0x05		2
644	322	34	RXMD4	0x04		2
642	321	33	RXMD5	0x05		3
640	320	32	RXMD4	0x04		3
63E	31F	31	RXMD5	0x05		4
63C	31E	30	RXMD4	0x04		4
63A	31D	29	RXMD5	0x05		5
638	31C	28	RXMD4	0x04		5
636	31B	27	RXMD5	0x05		6
634	31A	26	RXMD4	0x04		6
632	319	25	RXMD5	0x05		7
630	318	24	RXMD4	0x04		7
62E	317	23	RXMD3	0x03		2
62C	316	22	RXMD2	0x02		2
62A	315	21	RXMD3	0x03		3
628	314	20	RXMD2	0x02		3
626	313	19	RXMD3	0x03		4
624	312	18	RXMD2	0x02		4
622	311	17	RXMD3	0x03		5
620	310	16	RXMD2	0x02		5
61E	30F	15	RXMD3	0x03		6
61C	30E	14	RXMD2	0x02		6
61A	30D	13	RXMD3	0x03		7
618	30C	12	RXMD2	0x02		7
616	30B	11	RXMD1	0x01		2
614	30A	10	RXMD0	0x00		2
612	309	9	RXMD1	0x01		3
610	308	8	RXMD0	0x00		3
60E	307	7	RXMD1	0x01		4
60C	306	6	RXMD0	0x00		4
60A	305	5	RXMD1	0x01		5
608	304	4	RXMD0	0x00		5
606	303	3	RXMD1	0x01		6
604	302	2	RXMD0	0x00		6
602	301	1	RXMD1	0x01		7
600	300	0	RXMD0	0x00		7

	Second Bank of RX Threshold DACs (0:255 for 0 to 255 uA)					
VME	SetUp BUS	Data Stream	Technical Detail			
Add	ADDRESS	Number	RX MDAC #	MD_SEL	PAL	MD_SADD
6BE	35F	95	RXMD15	0x0F	RX_MDPAL1	2
6BC	35E	94	RXMD14	0x0E		2
6BA	35D	93	RXMD15	0x0F		3
6B8	35C	92	RXMD14	0x0E		3
6B6	35B	91	RXMD15	0x0F		4
6B4	35A	90	RXMD14	0x0E		4
6B2	359	89	RXMD15	0x0F		5
6B0	358	88	RXMD14	0x0E		5
6AE	357	87	RXMD15	0x0F		6
6AC	356	86	RXMD14	0x0E		6
6AA	355	85	RXMD15	0x0F		7
6A8	354	84	RXMD14	0x0E		7
6A6	353	83	RXMD13	0x0D		2
6A4	352	82	RXMD12	0x0C		2
6A2	351	81	RXMD13	0x0D		3
6A0	350	80	RXMD12	0x0C		3
69E	34F	79	RXMD13	0x0D		4
69C	34E	78	RXMD12	0x0C		4
69A	34D	77	RXMD13	0x0D		5
698	34C	76	RXMD12	0x0C		5
696	34B	75	RXMD13	0x0D		6
694	34A	74	RXMD12	0x0C		6
692	349	73	RXMD13	0x0D		7
690	348	72	RXMD12	0x0C		7
68E	347	71	RXMD11	0x0B		2
68C	346	70	RXMD10	0x0A		2
68A	345	69	RXMD11	0x0B		3
688	344	68	RXMD10	0x0A		3
686	343	67	RXMD11	0x0B		4
684	342	66	RXMD10	0x0A		4
682	341	65	RXMD11	0x0B		5
680	340	64	RXMD10	0x0A		5
67E	33F	63	RXMD11	0x0B		6
67C	33E	62	RXMD10	0x0A		6
67A	33D	61	RXMD11	0x0B		7
678	33C	60	RXMD10	0x0A		7
676	33B	59	RXMD9	0x09		2
674	33A	58	RXMD8	0x08		2
672	339	57	RXMD9	0x09		3
670	338	56	RXMD8	0x08		3
66E	337	55	RXMD9	0x09		4
66C	336	54	RXMD8	0x08		4
66A	335	53	RXMD9	0x09		5
668	334	52	RXMD8	0x08		5
666	333	51	RXMD9	0x09		6
664	332	50	RXMD8	0x08		6
662	331	49	RXMD9	0x09		7
660	330	48	RXMD8	0x08		7

Monitoring

VME Add	Addr	Read Function	Bits	Write Function	Label	Note
70A	385	ADC Data[11:8]	[0,0,0,0,D11,D10,D9,D8]	No Action	aMON_MSDAT	[4],[5]
708	384	ADC Data[7:0]	[D7:D0]	No Action	aMON_LSDAT	[4],[5]
706	383	No Action	Don't Care	No Action	aMON_SPARE	
704	382	No Action	Don't Care	ADC Convert	aMON_CONV	[3]
702	381	No Action	Channel Number (0-11)	ADC Config	aMON_FIG	[2]
700	380	No Action	Don't Care	ADC SetUp	aMON_SUP	[1]

Notes:

[1]	Write to this address to initialise the Monitor ADC chip - data is ignored.
[2]	Write Channel Number here to select which parameter will be converted (see below).
[3]	Write to this address to perform an ADC CONVERT: data ignored.
[4]	Read from these addresses to get the result of the last ADC CONVERT.
[5]	Series BOCs with HW_Rev = 0 have a 10-Bit ADC: for them, use Reading = [D9:D0,0,0]
[6] below	This is average of VPIN for streams[0:23] and VPIN for streams[24:47]: so get half expected v
[7] below	This is average of VPIN for streams[48:71] and VPIN for streams[72:95]: so get half expected

Channels:

Channel	Parameter		Formulae		Note
			BOC RevA	BOC RevB&C	
0	PIN Current	Stream[0:11]	1	4	
1	PIN Current	Stream[12:23]	1	4	
2	PIN Current	Stream[24:35]	1	4	
3	PIN Current	Stream[36:47]	1	4	
4	PIN Current	Stream[48:59]	1	4	
5	PIN Current	Stream[60:71]	1	4	
6	PIN Current	Stream[72:83]	1	4	
7	PIN Current	Stream[84:95]	1	4	
8	PIN Voltage	Stream[0:47]	2	5	[6]
9	PIN Voltage	Stream[48:95]	2	5	[7]
10	Thermistor 1		3	6	
11	Thermistor 2		3	6	

Formulae:

RevA/ RevB	Formula Number	Formula Form	Parameter Values K	Parameter Values M	Range Max	Nominal Value
RevA	1	K + M*Reading	41520 uA	-10.147 uA/ct	41.52 mA	
	2	M*Reading		2.777 mV/ct	11.36 V	8.42 V
	3	RTherm = K*((M/Reading) -1)	10000 Ohm	4095		10K @ 25
RevB & RevC	4	K + M*Reading	-97 uA	5.958 uA/ct	24.375 mA	
	5	M*Reading		3.623 mV/ct	14.83 V	9.78 V
	6	RTherm = K*((M/Reading) -1)	10000 Ohm	4095		10K @ 25

Getting Temperature from RTherm:

Thermistor Used	ATC Semitec 103KT1608 to VADC with 10K to ground		
Steinhart-Hart Formula	1/T (Kelvin) = C0 + C1*ln(RTherm) + C3*(ln(RTherm))**3		
Parameters Optimised over 20 - 100 Deg C	RevA	C0	7.4717E-04
		C1	2.7726E-04
		C3	6.8388E-08
	RevB & RevC	C0	7.4717E-04
		C1	2.7726E-04
		C3	6.8388E-08

BOC Controls

VME Add	Addr	Read Function	Bits	Write Function	Label	Note
7BE	3DF					
7BC	3DE					
79A	3CD					
7B8	3DC					
7B6	3DB					
7B4	3DA					
7B2	3D9					
7B0	3D8	Serial No. (board switches)	[7:0]	No Action	MOD_SN	
7AE	3D7					
7AC	3D6					
7AA	3D5					
7A8	3D4					
7A6	3D3	Manufacturer = CB (hex)	[7:0]	No Action	MANUF	
7A4	3D2	Module Type = 46 (dec)	[7:0]	No Action	MOD_TYPE	[1]
7A2	3D1	Hardware Revision	[7:0]	No Action	HW_REV	[2]
7A0	3D0	Firmware Revision	[7:0]	No Action	FIRM_REV	
79E	3CF					
79C	3CE					
79A	3CD					
798	3CC					
796	3CB					
794	3CA	Clock Control Bits	[4:0]	Clock Control Bits	CK_CONT	[3]
792	3C9	Reserved		Reserved		
790	3C8	Vernier Clock Fine Phase	[7:0]	Vernier Clock Fine Phase	VC_FPh	[4]
78E	3C7					
78C	3C6					
78A	3C5	RX Data Mode	[2:0]	RX Data Mode	RXDMODE	[7]
788	3C4	BOC Status	[7:0]	No Action	BOCSTAT	[5]
786	3C3					
784	3C2					
782	3C1					
780	3C0	BOC Reset	[7:0]	BOC Reset	BOCRST	[6]

Notes:

[0] ROD should support access to the whole range 3c0-3df hex - they may be used by later revisions

[1] Module type is 46 for RevA and RevB BOCs. Prototype BOCs were type 44

[2] Harware Revision is 1 for RevA, and Currently 2 for RevB: this may increment

[3] Clock Control word: [P4_DIV4,BPMPh_Bypass,VernierStep_Bypass,Half_Clock,Clock_Invert]

[4] Vernier Clock Fine Phase: [7:0] sets delay in 40ps steps (0-10ns)

[5] BOCSTATUS [REM_LAS_EN,LOC_LAS_EN,ROD_SENSE,ERR_FLAG,VA_OK,VB_OK,BOC_OK_REG,x]

[6] BOC_Reset [BPMRESET,TXD_CLR,RXD_CLR,VPIN_RST,BOC_OK_REG_PRESET,x,x,x]

[7] RX Modes:

Mode#	Action
0	SCT Normal (B-Reg)
1	SCT Timing (B- & V-Reg)
2	Pixel Layer 2 (40Mb/s remapped)
3	Pixel Layer 1 & B (80 Ms/s remapped)
4	"AND" reference clocks (test mode)
5	"OR" reference clocks (test mode)
6	Clock as Data (test mode)
7	Transparent

BOC-Rig2 Registers (BOC-Rig2 is the Front-of-Crate Module used to exercise BOC in the lab)			
VME ADDRESS	Read/Write	Function	Notes
820			
81E		Reserved	
81C		Reserved	
81A		Reserved	
818	R	Firmware Version	
816	R	Manufacturer MS	
814	R	Manufacturer LS	
812	R	Module Version	
810	R	Module Type	
80E	RW	Scope Mode delay counter [7:0]	
80C	RW	LEDs register [3:0]	
80A	R	[0,0,0,0,Snap[11:8]]	
808	R	Snap[7:0]	
806	W (any Data)	Write here for Data Snapshot	1
804	RW	[0,0,0,0,0,RSEL2,RSEL1,RSEL0]	
802	RW	[0,0,0,0,0,0,LASE,COMMINV,PIXEL8]	
800	RW	[0,0,0,0,0,0,0,0,BUSY] // Reset	2

NOTES

1 also step Shift Reg in Scope Mode

2 Reset - Scope Mode only

Revision Record		
Date	**Sheets Affected**	**Note**
29-Aug-03		Updated for BOC_Series - for both RevA and RevB
04-Nov-03	Monitoring, Controls	Updated
05-Dec-03	RIG2	BOC-RIG2 Address Map added
27-Feb-04	Monitoring	Modified to work with 12-Bit ADC (as well as 10-Bit ones)
13-Mar-06	BOC Controls	Added details for extra register contents

Notes	
Sheets Affected	**Note**